APPLICATION NOTE U-157

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FUELING THE MEGAPROCESSOR - A DC/DC CONVERTER DESIGN REVIEW FEATURING THE UC3886 AND UC3910

UNITRODE

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ABSTRACT

This application note provides a detailed account of design tradeoffs and procedures for the development of a Voltage Regulator Module (VRM) for the Intel Pentium®Pro processor. This voltage regulator features Unitrode's UC3886 Average Current Mode PWM Controller and UC3910 4-BIT DAC and Voltage Monitor ICs configured in a Buck Regulator. Test results and waveforms are provided which show how the VRM power supply meets stringent requirements imposed by Intel.

INTRODUCTION

Intel's Pentium®Pro power system specification demonstrates the industry trend to operate at lower voltages and at higher currents, with tight regulation and fast transient response. Meeting these requirements demands the most of both the power stage and the control system of the power supply. Unitrode's UC3886 and UC3910 are specifically designed for optimizing the control loop, the dynamic response and the DC accuracy required by the Pentium®Pro. The power stage inductor and capacitors are critical as well in meeting the extremely tight voltage regulation during a Pentium®Pro load transient.

This application note will detail the design of a complete VRM power supply. This design review will detail the critical VRM specifications, power supply architecture tradeoffs, power stage design details and equations and finally design specifics used to configure the UC3886 and UC3910. The complete current and voltage loops will then be closed, and performance results of the power supply will be shown.

This design review will reveal the many advantages of using the UC3886 and UC3910, which include:

- Direct output NMOS drive, eliminating the need for creating high voltages and allowing the use of an efficient N-Channel MOSFET.
- High DC accuracy negates the need for voltage trimming and insures the overall regulation will be met.
- Direct interface with INTEL's PENTIUM™ PRO VID programming codes.
- The UC3910's DAC and unique voltage monitoring architecture directly replaces discrete components including a precision reference, a DAC, complicated resistive networks, multiple window comparators and an SCR Driver.
- Accurate and true "square-knee" current limiting eliminates the need to over-design the power components for operation in an indefinite short circuit.
- Optimization of the loop performance due to large signal changes due to transient loading effects.

The Unitrode VRM demonstration kit is shown in Figure 1. The VRM's schematic is shown in Figure 2 and the parts are described in Table 1.

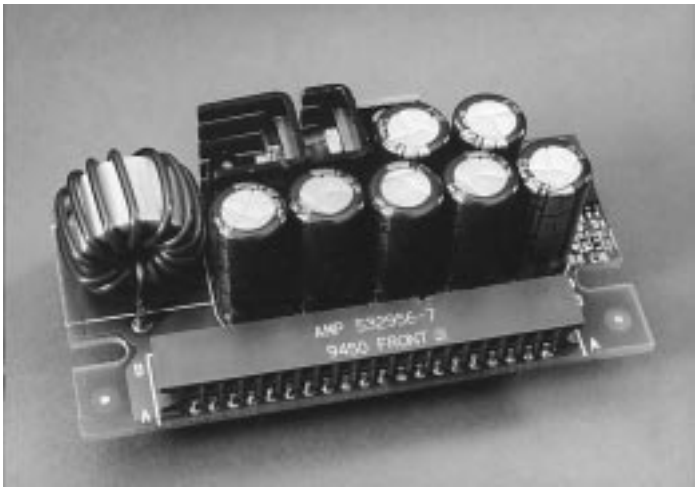

Figure 1. Unitrode's VRM Demonstration Kit

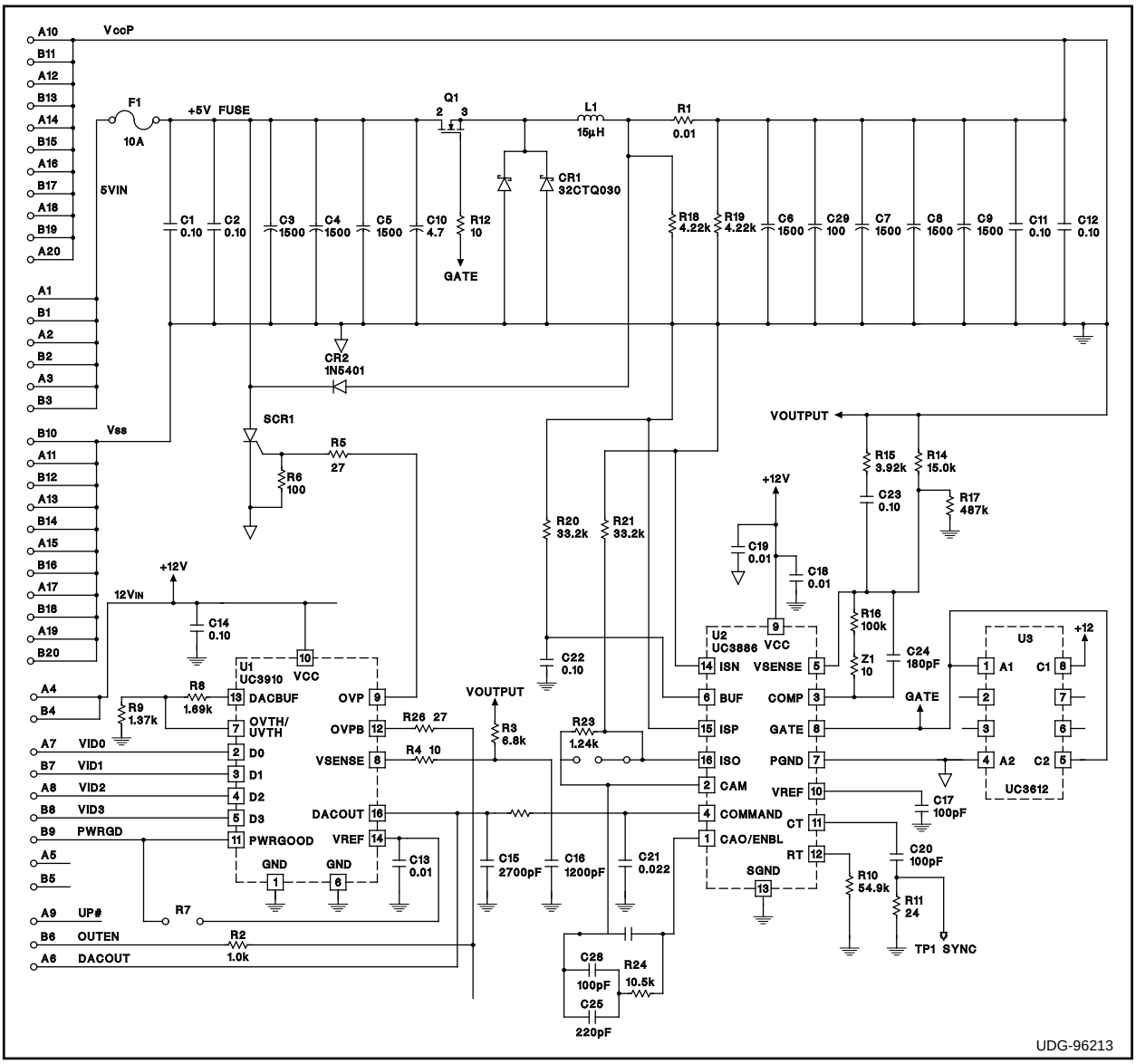

Figure 2. Schematic Diagram

POWER SUPPLY SPECIFICATIONS

The requirements for the DC/DC converter which will provide power to Intel Pentium®Pro are contained in Intel's application note AP-523 [1], Section 10. These power supply requirements consist of required specifications, expected specifications and design guidelines, some of which are summarized below.

Input Voltages: 5.00V ±5%
12.00V ±5%

Output Voltage: Variable from 2.4V to 3.4V programmable per INTEL VID codes, 100mV increments.

Minimum Current: 0.3A

Maximum Current: 11.2A

Regulation: ±5% Including initial tolerance, setpoints, drift, transients and ripple/noise.

Load Transient: Minimum to maximum or maximum to minimum current at a rate ≤30.3A/µs.

Input Current Rate: ±0.1A/µs maximum during a load transient.

Power-Good: Open Collector output LOW signal when the output voltage is not within ±10% of nominal.

Output Enable: Open Collector input signal with a LOW state disabling the DC/DC converter.

Ripple/Noise: ±1% to 20MHz.

Overshoot: ≤10% above the initial setpoint at application or removal of input power.

Efficiency: ≥80% at maximum current, ≥40% at minimum current

Temperature: +10°C to +60°C, ≥100 LFM air cooling along connector axis.

Over Voltage: Self shut down when the output exceeds 10% to 20% of nominal.

Short Circuit: Continuous short circuit mode-without damage or overstress to the unit.

TABLE 1 - PENTIUM®PRO VRM DEMONSTRATION KIT BILL OF MATERIALS

UNITRODE PENTIUM®PRO VRM DEMONSTRATION KIT			
REF.DES.	**DESCRIPTION**	**PACKAGE**	**NOTES**
U1	Unitrode UC3910DP 4-BIT DAC and Voltage Monitor	SOIC-16	
U2	Unitrode UC3886DP ACM PWM Controller	SOIC-16	
U3	Unitrode UC3612DP Dual Schottky Diode	SOIC-8	
C01	0.10µF Ceramic	1206 SMD	
C02	0.10µF Ceramic	1206 SMD	
C03	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C04	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C05	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C06	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C07	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C08	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C09	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C10	Sprague/Vishay 595D475X0016A2B, 4.7µF 16V Tantalum	SPRAGUE Size A	
C11	0.10µF Ceramic	1206 SMD	
C12	0.10µF Ceramic	1206 SMD	
C13	0.10µF Ceramic	1206 SMD	
C14	0.10µF Ceramic	1206 SMD	
C15	2700pF Ceramic	0603 SMD	
C16	1200pF Ceramic	0603 SMD	
C17	1000pF Ceramic	0603 SMD	
C18	0.01µF Ceramic	0603 SMD	
C19	0.10µF Ceramic	1206 SMD	
C20	100pF NPO Ceramic	0603 SMD	
C21	0.022uF Ceramic	0603 SMD	
C22	0.10µF Ceramic	1206 SMD	
C23	0.10µF Ceramic	1206 SMD	

TABLE 1 - PENTIUM®PRO VRM DEMONSTRATION KIT BILL OF MATERIALS (cont.)

REF.DES.	DESCRIPTION	PACKAGE	NOTES
C24	180pF NPO Ceramic	0603 SMD	
C25	220pF NPO Ceramic	0603 SMD	
C26	NOT USED	0603 SMD1	
C27	180pF NPO Ceramic	0603 SMD	
C28	1000pF NPO Ceramic	0805 SMD	
C29	Sprague/Vishay 593D107X9010D2, 100µF, 6.3V Tantalum	EIA Size D SMD	
SCR1	Motorola MCR12D, 12A SCR	TO-220AB	2
CR1	International Rectifier 32CTQ030 30V, 30A Schottky Diode	TO-220AB	
CR1-HS	AAVID 577002 TO-220 Heat Sink		
CR2	1N5401CT, 3A 100V Diode	DO-201AD	2
F1	Littlefuse R451010, 10A Fast Blow	SMD Square	2
J1	AMP 532956-7 40 Pin Connector		
L1	Coilcraft S6030-B, 10µH to 20µH	Radial Toroid	
Q1	International Rectifier IRL3103, 30V, 56A	TO-220AB	
Q1-HS	AAVID 577202 TO-220 Heat Sink		
R01	Dale/Vishay WSR-2 0.01W 1%	SMD Power Package	3
R02	1.00kW, 1%, 1/16 Watt	0603 SMD	
R03	6.8kW, 5%, 1/16 Watt	0603 SMD	
R04	10W, 5%, 1/16 Watt	0603 SMD	4
R05	27W, 5%, 1/16 Watt	0603 SMD	2
R06	100W, 5%, 1/16 Watt	0603 SMD	2
R07	NOT USED	0603 SMD	5
R08	1.69kW, 1%, 1/16 Watt	0603 SMD	
R09	1.37kW, 1%, 1/16 Watt	0603 SMD	
R10	54.9kW, 1%, 1/16 Watt	0603 SMD	
R11	24W, 5%, 1/16 Watt	0603 SMD	8
R12	10W, 5%, 1/16 Watt	0603 SMD	
R13	10kW, 5%, 1/16 Watt	0603 SMD	
R14	15.0kW, 1%, 1/16 Watt	0603 SMD	
R15	3.92kW, 1%, 1/16 Watt	0603 SMD	
R16	100kW, 1%, 1/16 Watt	0603 SMD	
R17	487kW, 1%, 1/16 Watt	0603 SMD	
R18	4.22kW, 1%, 1/16 Watt	0603 SMD	
R19	4.22kW, 1%, 1/16 Watt	0603 SMD	
R20	33.2kW, 1%, 1/16 Watt	0603 SMD	
R21	33.2kW, 1%, 1/16 Watt	0603 SMD	
R22	NOT USED	0603 SMD	1
R23	1.24kW, 1%, 1/16 Watt	0603 SMD	
R24	10.5kW, 1%, 1/16 Watt	0603 SMD	
R25	NOT USED	0603 SMD	
R26	27W, 5%, 1/16 Watt	0603 SMD	6
Z1	10W, 5%, 1/16 Watt	0603 SMD	7

Notes:
1) R22 and C26 are not required. These parts can be used for alternative compensation schemes.
2) These parts are related to the overvoltage protection SCR firing circuit.
3) Simulate a ”4 wire” connection using PCB etch for best results.
4) R04 used for debug purposes. R04 is not required in a production unit.
5) R07 can be used to pull up the PWRGOOD signal internally to the VRM
6) R26 is not required for proper operation. R26 is used as a ”jumper”.
7) Z1 used for debug purposes. Z1 can be used for alternative compensation, or shorted in a production unit.
8) R24 is not required for production unless synchronization is used.

POWER CONVERSION ARCHITECTURE

Topology: Single Switch Buck Regulator

Power conversion from either +5 volts or +12 volts to the lower voltages required by the Pentium®Pro can be accomplished by either a linear regulator or by a myriad of switching converter topologies. Linear regulation is not appropriate because of its inherently poor efficiency. Transformer coupled switching topologies are not required, and not desired, because of the common input and output grounding system. Either a single switch or a synchronous rectifier (two switch) buck regulator are the most appropriate choices for this application. Higher efficiency can be achieved with synchronous rectification, but is not required in this application because the efficiency goal is 80%. The added cost and complexity of a second N-MOSFET is therefore not justified.

Input Voltage: +5 Volts Provides Power, +12 Volts provides Bias and Drive

Either the +5 volt or the +12 volt power bus can be used for this single switch Buck regulator. An N-channel MOSFET is chosen as the switch because of the efficiency of low R_{DSon} N-MOSFETs. The +12 volt bus can be used to drive the N-MOSFET in a +5V input Buck regulator, whereas a +12V input Buck regulator would require a higher voltage (17-20 volts) to provide drive to the switch. Several other considerations are made in choosing the input voltage, including:

- +12V input would require a larger output inductor for a given ripple current.
- +5V input operates at higher duty cycles, reducing power in the freewheeling diode, whereas +12V input operates at lower duty cycles, reducing power in the MOSFET.
- The combined power dissipated of the freewheeling diode plus the MOSFET is less with a +5V input than with a +12V input.
- +5V typically has better power distribution on a motherboard, and within a system, even considering the higher DC currents involved when converting power from +5V.
- The input capacitors will see the same RMS switching current at either voltage.
- +5V has six dedicated input pins whereas +12V has only two. Using +5V as an input voltage will result in fewer amps/pin and a lower impedance path to the source.
- +12V busses can often withstand larger voltage deviations due to the loading effects of the Pentium®Pro.

Control Method - Average Current Mode Control Using the UC3886

Average Current Mode control, as implemented with the UC3886, offers the advantages of optimization of the control loop, very fast amplifiers for a fast transient response, and accurate current limiting. Application Note U-140 [2] discusses the many advantages of Average Current Mode control over both Peak Current Mode control and Voltage Mode control.

Switching Frequency - 200kHz

Several considerations in choosing 200kHz as the switching frequency are:

1. An upper bound on frequency is derived from the gain required by the UC3886 Average Current Mode control current sense amplifier. This upper bound will be shown to be 312kHz.
2. A high switching frequency is desired for
   - Minimum output inductor size
   - Maximum control loop bandwidth
3. A low switching frequency is desired for
   - Keeping switching losses low, although switching losses in the semiconductors is not a significant factor in this application because the input voltage (+5V) is very low.
   - Reducing noise when using a 2-layer printed circuit board.
4. The use of Aluminum Electrolytic capacitors is favored for both input and output capacitors in this application because of the height allowed, their high Capacitance-to-ESR and Capacitance-to-ESL ratios and their ripple current capabilities. Surveying several suppliers of Aluminum Electrolytic capacitors revealed that they have significantly low impedance and optimal ripple current handling at 100kHz to 200kHz, where ESR is minimal.

POWER STAGE COMPONENT SELECTION

The power stage components consist of the input and output capacitors, switch, freewheeling diode, output inductor and sense resistor, and are chosen to be leaded devices for the most part because of the height allowed in this design. The semiconductors are first chosen to meet a full load efficiency goal of 80% and to provide reliable operation at full load. The output inductor is then chosen to provide low output current ripple into the capacitors and for continuous mode operation of the

Buck regulator. The output capacitors are chosen to provide an extremely low output impedance for low voltage ripple and low voltage droop during and output load transient. Finally, the input capacitors are chosen to handle the high level of ripple current demanded by the Buck regulator and to heavily filter the input voltage from both high and low load transients.

Efficiency/Power Dissipation Budget

The desired efficiency goal of ≥80% at full load operation will govern how many of the power stage components are selected. Efficiency goals are set at a nominal input voltage of +5.00V, an output voltage of 3.1V, +25°C ambient temperature and at a maximum load current of 11.2A.

The nominal output power of the power supply is equal to 3.1V • 11.2A = 34.72 Watts. From the desired efficiency, the input power at full load is

$$P_{IN} = \frac{P_{OUT}}{0.8} = \frac{34.72W}{0.8} = 43.4 \text{ Watts}$$

The power dissipated is 8.68 Watts, at full load. An example efficiency budget is shown in Table 2.

Power Stage Component Design Details

Freewheeling Diode: CR1

International Rectifier 32CTQ030 or equivalent, 2 legs paralleled

$V_F \approx 0.35V$ @ $T_J = 115°C$

$T_{Jmax} = 150°C$

Heat Sink = AAVID P/N 577002 or equivalent

Low voltage schottky technology is chosen to maximize the efficiency of the power supply, based on its lower forward voltage and lack of reverse recovery losses.

The operating duty cycle for this Buck converter is derived based on the equation[3]

$$D = \frac{V_O + I_O \bullet (R_{SENSE} + R_{LOUT}) + V_F}{V_{IN} - (I_O \bullet R_{DSon}) + V_F}$$

Likewise, the short circuit operating duty cycle is given by

$$D_{SC} = \frac{0.0V + I_{SC} \bullet (R_{SENSE} + R_{LOUT}) + V_F}{V_{IN} - (I_{SC} \bullet R_{DSon}) + V_F}$$

Given R_{SENSE} = 0.01

R_{LOUT} = 0.012 at 25°C, full load current

V_F = 0.35V at full load, 0.25 at minimum load

I_{SC} = 12.5A Nominal Short Circuit Current

V_{IN} = 5.00V Nominal

R_{DSon} = 0.025 at 110°C

V_O = 3.10V Nominal

Then typical duty cycles will be approximately:

Operating: ≈ 73% at Full load, 25°C T_A

≈ 64% at minimum load, 25°C T_A

Short Circuit: ≈ 13%

The maximum operating power dissipation at the diode's maximum operating junction temperature of 110°C is given by

$$P_{Dmax} = V_F \bullet I_{Omax} \bullet (1 - D_{max})$$
$$= 0.35V \bullet 11.2A \bullet (1 - 0.73) = 1.06W$$

The power dissipation under short circuit conditions, however, is substantially larger

$$P_{Dsc} = V_F \bullet I_{sc} \bullet (1 - D_{sc}) = 0.35V \bullet 1.12A \bullet (1 \bullet 0.73) = 1.06W$$

Let T_{Jmax} = 115°C under operating conditions and 150°C under short circuit conditions (Rated T_{Jmax} for device)

The two governing formulas defining the heat sink requirements (thermal impedance RθHS) are

115°C = 50°C + 1.06W • (3.0 + RθHS), RθHS = 58°C/W

150°C = 50°C +3.80W • (3.0 + RθHS), RθHS = 23.3°C/W

The short circuit operation must be used to choose the heat sink. AAVID P/N 577002 with 100LFM of airflow meets the heat sink requirement of ≤23°C/W. Note that the accurate current limit set

TABLE 2 - POWER DISSIPATION BUDGET

Description	Power Dissipated [W]	Budget Remaining [W]
Budgeted Power		8.68
Estimated 3% Power Distribution (I^2R) Losses	1.1	7.58
Diode Losses	1.1	6.48
Sense Resistor	1.25	5.23
Output Inductor (I^2R)	1.3	3.93
Output Inductor (Core)	0.1	3.83
Input Capacitance Ripple Current Losses	0.5	3.33
UC3886 + UC3910 + Bias loads	0.3	3.03
MOSFET (Switching, Conduction, Gate Drive)	3.03	0.00

point achieved by the UC3886 allows for a minimum heat sink solution.

MOSFET Switch: Q1

International Rectifier IRL3103

$R_{DSon} \approx 0.025\Omega$ Estimated at V_{GS} = 7V, T_J = 115°C

Q_G (Total Gate Charge) ≈ 50nC estimated at V_{GS} =7V

Heat Sink ≈ AAVID P/N 577202 or equivalent

From the power budget, the MOSFET should be chosen to achieve the desired losses, including the gate drive losses. Choosing a Logic Level MOSFET or a standard threshold voltage MOSFET is discussed in U-156 [3]. This application will utilize a Generation 5 MOSFET from International Rectifier because of its combination of low R_{DSon} at low V_{GS} as well as rated V_{GS} of ±20V.

The power dissipation of the MOSFET consists of 4 components; (a) Gate drive, (b) C_{OSS}, (c) Crossover losses, and (d) Conduction losses

a) Gate Drive losses are given by

$$P_{GATE} = I_{GATEavg} \bullet V_{GS}$$

From the IRL3103 charge curve, with V_{GS} = 7 volts, the required total charge, Q_G, is estimated to be 50nC. The average current is given by

$$I_{GATEavg} = Q_G \bullet F_S = 50nC \bullet 200kHz = 10mA$$

$$P_{GATE} = 0.010 \text{ Amps} \bullet 12 \text{ Volts} = 0.12 \text{ Watts}$$

b) Coss losses are due to the discharge of the energy stored in the capacitance Coss each cycle, equivalent to

$$P_{COSS} = 0.5 \bullet Coss \bullet (V_{IN} + V_F)^2 \bullet F_S$$

From the IRL3103 capacitance curve, Coss is estimated to be 2400pF. Therefore,

$$P_{COSS} = 0.5 \bullet 2400pF \bullet (5.35V)^2 \bullet 200kHz = 0.007W.$$

c) Crossover (turn-on and turn-off) losses can be estimated as

$$P_{CROSSOVER} = \frac{1}{6} \bullet (V_{IN} + V_F) \bullet I_O \bullet \frac{T_{RISE/FALL}}{T_S}$$

where $T_{RISE/FALL}$ is the MOSFET current rise and fall time, estimated to be approximately 150ns, and T_S is the switching period. This loss occurs once at turn-on, and once at turn-off, and therefore, for this application

$$P_{CROSSOVER} = 2 \bullet \frac{1}{6} \bullet 5.35V \bullet 11.2A \bullet \frac{150ns}{5\mu s} = 0.6 \text{ Watts}$$

d) Conduction losses are determined by

$$P_{COND} = I_O^2 \bullet R_{DSon} \bullet D_{MAX}$$

and are worst at the maximum operating junction temperature, where R_{DSon} is highest. For the IRL3103, this loss is

$$P_{COND} = 11.2^2 \bullet 0.025\Omega \bullet 0.73 = 2.29 \text{ Watts}$$

Pd_Total_FET = 2.29W + 0.6W + 0.007W + 0.12W = 3.02W

The MOSFET heat sink requirements are determined from

$$115°C = 50°C + 3.02W \bullet (2.0 + R_{\theta HS}),$$

$R_{\theta HS}$ = 19.5°C/W

AAVID P/N 577202 with 100LFM of airflow provides ≤14°C/W, exceeding the heat sink requirement.

Output Inductor: L1

Coilcraft P/N S6030-B

20µH @ 0 Adc

10µH @11.2 Adc

13 Turns, # 16AWG on Micrometals T60-52D Core

$R_{DC} \leq 0.008\Omega$ max, 20°C Ambient

$T_{RISE} \approx 40°C$ at maximum load

The output inductor of a Buck regulator is often chosen to maintain continuous current in the inductor under minimum load conditions. The ripple current in the inductor under minimum DC current conditions is equal to 2 • I_{MIN} for this rule to apply. For this power supply, L_{OUT} is determined by

$$L_{OUT} = \frac{(V_{IN} - V_{OUT}) \bullet Duty}{2 \bullet I_{MIN} \bullet F_S} = \frac{(5V - 3.1V) \bullet 0.64}{2 \bullet 0.3A \bullet 200kHz} = 10.1\mu H \text{ @ Low Load}$$

A second condition for choosing the output inductor value is to limit the input current to the power supply during a step change in current from I_{MIN} to I_{MAX}. After a step change in load current, the duty cycle of the Buck regulator responds by assuming a maximum duty cycle of 100%. The input current therefore equals the output inductor current. To limit the input current rate to the required 0.1A/µs, the output inductor is chosen by

$$L_{OUT} = \frac{(V_{IN} - V_{OUT})}{di/dt} = \frac{(5V - 3.1V)}{0.1A/\mu s} = 19\mu H$$

A toroidal inductor design is used to meet these needs. The form factor allows a component height of 0.800", thus allowing a sizable inductor that can be designed for low cost and simple winding techniques. The inductance vs DC current is shown in Figure 3. The inductor must not saturate with DC

current equal to the power supply short circuit current limit, or the current limiting will not be effective.

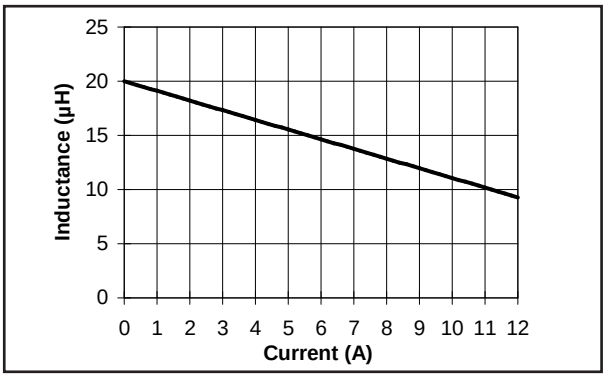

Figure 3. Output Inductor Performance vs DC Current - No AC Flux

The in-circuit inductance will tend to be higher due to the AC Flux imposed by the volt-seconds product of the Buck regulator. Micrometals -52 material's permeability increases substantially with AC Flux. This same effect of AC Flux on the permeability of the -52 material plays a major role during the transient load response of the power supply. During a transient load response, the voltage differential across the output inductor is approximately V_{IN}-V_{OUT}. The duration of the transient response, in excess of 100µs, means that the AC Flux on the core for this time is given by

$$\Delta B_{AC} = \frac{(V_{IN} - V_{OUT}) \bullet T_{LOUT} \bullet 10^8}{N \bullet Ae}$$

$$= \frac{(5V - 3.1V) \bullet 100\mu s \bullet 10^8}{13Turns \bullet 0.374\ cm^2}$$

$$= 3908\ Gauss$$

which, according to Micrometals [3] results in multiplying the output capacitance by approximately 260%. This results in a dynamic inductance, during a load step, of approximately 26µH. This feature will play an important role in the selection of the output capacitors to meet the transient load performance.

Output Capacitors: C06-C09, C11, C12, C29

SANYO - 6MV1500GX - 4 in Parallel

C = 1500µF

Form Factor = 10x20mm, Radial

ESR = 0.044Ω

ESL ≈ 4nH (Estimated)

Ripple Current Rating = 1.25A @ 105°C, 100kHz

Choosing the output capacitors for this regulator may be the single most important decision with regards to meeting the transient load behavior of the Pentium®Pro. The transient load step of the Pentium®Pro is so large and so fast that there is no control loop which can respond quickly enough and maintain regulation. Capacitance, providing a low impedance output, is therefore the best solution to maintaining the proper output voltage.

Understanding the Response to a Step Load

During a step load change from minimum to maximum current, the output of the power supply can be modeled as shown in Figure 4. Prior to the change in load current, the average current in the output inductor is I_{MIN} and the average current in the output capacitor is 0 amperes. Once the load current changes from Imin to I_{MAX}, the parasitic components shown in Figure 4 have a large affect on the output voltage.

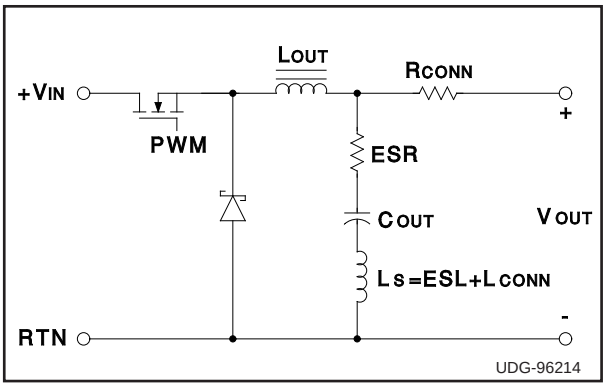

Figure 4. Large Signal Transient Model of Power Supply Output Stage

The VRM connector pins have parasitic resistance and inductance termed R_{CONN} and L_{CONN}. The parasitic inductance of the connector and the output capacitors (ESL) are summed together as L_S. ESR and R_{CONN} cannot be combined in the capacitor path as this would result in a DC load regulation error.

Figure 5 below illustrates the complexity of the output voltage waveform during a step in the output load current. A power supply with excellent load regulation is assumed for the purposes of understanding these dynamics. Reducing the load regulation through non-integrating [3] voltage loop gain will be discussed later in this application note. The output voltage responds to the load current step in four distinct phases, T_{STEP}, T_{LOOP}, T_{LOUT} and T_{CHARGE}.

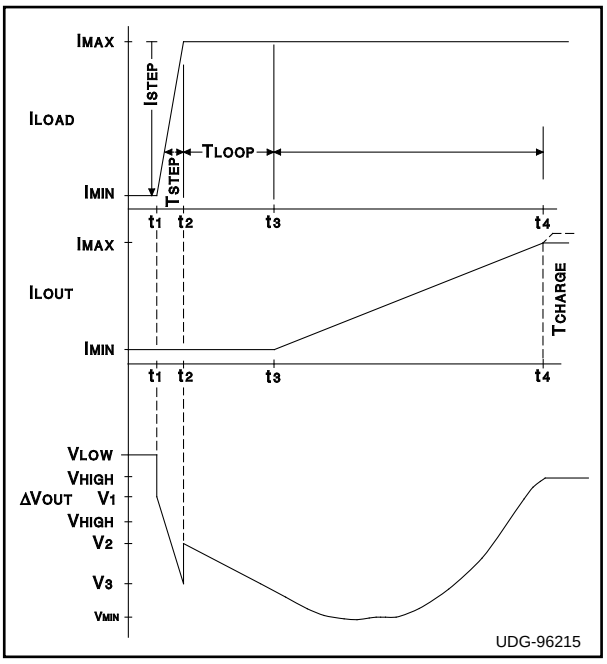

Figure 5. Dynamics of a Step Load

Phase 1, the step current phase from t_1 to t_2 (T_{STEP}), is characterized by a specified change in current and rise time. The response of the output voltage consists of:

a) A voltage step proportional to the parasitic circuit inductance, L_S.
b) A ramp in voltage proportional to the parasitic circuit resistance, R_S, where $R_S = R_{CONN} + ESR$.
c) A droop in voltage proportional to the power supply output capacitance.

The response of the output voltage during the time t_1 to t_2 is therefore given by

$$\Delta V_{OUT} = L_S \bullet \frac{\Delta I}{\Delta T} + i(t) \bullet R_S + \frac{1}{C_{OUT}} \int_{t_1}^{t_2} i(t)dt$$

which, at the end of T_{STEP}, is equal to

$$\Delta V_{OUT} = I_{STEP} \bullet \left(\frac{L_S}{T_{STEP}} + \frac{T_{STEP}}{2 \bullet C_{OUT}} + R_S \right)$$

Phase 2, from t_2 to t_3 (T_{LOOP}), is the time where the load current has settled at its maximum value, I_{MAX}, but the power supply loop has not yet responded. The inductor current is therefore still set at I_{MIN} and the response of the output voltage is therefore determined by

a) A voltage proportional to R_S.
b) A droop in voltage proportional to the power supply output capacitance.

There is an initial discharge of the capacitor at the end of Phase 1 which is the initial condition for Phase 2, determined by

$$\Delta V\_Phase1 = \frac{1}{C_{OUT}} \int_{t_1}^{t_2} \frac{I_{STEP}}{T_{STEP}} \bullet t \, dt$$

$$= \frac{I_{STEP} \bullet T_{STEP}}{2 \bullet C_{OUT}}$$

The response of the output voltage during the time t_2 to t_3 is therefore given by

$$\Delta V_{OUT} = \frac{I_{STEP} \bullet T_{STEP}}{2 \bullet C_{OUT}} + \frac{1}{C_{OUT}} \int_{t_2}^{t_3} i(t)dt + R_S \bullet$$

$$I_{STEP} = I_{STEP} \bullet \left(\frac{T_{STEP}}{2 \bullet C_{OUT}} + \frac{T_{LOOP}}{C_{OUT}} + R_S \right)$$

T_{LOOP}, for the UC3886 Average Current Mode Controller and the compensation components shown in Figure 2, is less than one switching cycle.

Phase 3, from t_3 to t_4 (T_{LOUT}), is the time when control loop has forced the Buck regulator to the maximum duty cycle (100% for the UC3886) and the inductor current is ramping from I_{MIN} to I_{MAX}. The output inductor current during this phase is given by

$$iL_{OUT(t)} = \frac{(V_{IN} - V_{OUT})}{L_{OUT}} \bullet t$$

Since the inductor current is ramping up during Phase 3, the capacitor current is ramping down, and is given by

$$iC_{OUT(t)} = I_{STEP} - IL_{OUT(t)}$$

$$= I_{STEP} - \frac{(V_{IN} - V_{OUT})}{L_{OUT}} \bullet t$$

The change in output voltage during Phase 3 consists of

a) A voltage drop proportional to ESR and R_{CONN}.
b) A droop in voltage proportional to the output capacitance.

During Phase 3, the voltage drop due to the ESR and the capacitance is changing because the capacitor current decreases. The voltage drop due to R_{CONN} is constant, as it is set by the constant value of R_{CONN} and the maximum load current, I_{STEP}. There is an initial discharge of the capacitor at the end of Phase 2 which is the initial condition for Phase 3, determined by

$$\Delta V\_Phase2 = \frac{1}{C_{OUT}} \int_{t_1}^{t_2} \frac{I_{STEP}}{T_{STEP}} \bullet t \, dt + \frac{1}{Cout}$$

$$\int_{t_2}^{t_3} I_{STEP} \, dt = \left(\frac{Istep}{2} \right) \bullet \left(\frac{2 \bullet T_{LOOP} - T_{STEP}}{C_{OUT}} \right)$$

The change in output voltage during Phase 3 is given by

$$\Delta V_{OUT} = \left(\frac{I_{STEP}}{2}\right) \bullet \left(\frac{2 \bullet T_{LOOP} - T_{STEP}}{C_{OUT}}\right) + \frac{1}{C_{OUT}} \int_{t_3}^{t_4} iC_{OUT(t)}dt + iC_{OUT(t)} \bullet ESR + I_{STEP} \bullet R_{CONN}$$

Which yields

$$\Delta V_{OUT} = \left(\frac{I_{STEP}}{C_{OUT}}\right) \bullet \left(t - \frac{T_{STEP}}{2} + T_{LOOP} - \frac{t^2}{2 \bullet T_{LOUT}}\right) + I_{STEP} \bullet \left(EST - \frac{ESR \bullet t}{T_{LOUT}} R_{CONN}\right)$$

T_{LOUT} is defined as the time it takes for the inductor current to equal the change in load current, I_{STEP}.

$$T_{LOUT} = \left(\frac{I_{STEP}}{(V_{IN} - V_{OUT})}\right) \bullet L_{OUT}$$

Phase 4, T_{CHARGE}, is the time when the inductor current overshoots to reach the programmed short circuit current limit in order to replace charge lost by the output capacitor. At the end of phase 4, the output voltage drop settles to

$$\Delta V_{OUT} = I_{STEP} \bullet R_{CONN}$$

The duration of phase 4 is determined by

$$I_{Cout} = C_{OUT} \bullet \frac{dv}{dt}$$ which yields a time of

$$T_{CHARGE} = \frac{C_{OUT} \bullet \Delta V\_Phase3}{(I_{SC} - I_{MAX})}$$

where I_{SC} is the programmed short circuit current limit, and ΔV_Phase3 is the voltage at the end of phase 3, determined by

$$\Delta V\_Phase3 = \frac{I_{STEP}}{C_{OUT}} \bullet \left(\frac{T_{LOUT}}{2} - \frac{T_{STEP}}{2} + T_{LOOP}\right)$$

Procedure for Determining the Required Output Capacitor(s)

Step 1: Determine the parasitic values of R_{CONN} and L_{CONN}. The following are estimates based on the connector pair used and the printed circuit board.

Resistance per pin ≈ 10mΩ

Resistance per mated pin set ≈ 20mΩ

Inductance per mated pin set ≈ 4.28nH

Number of output pins = 11 pairs in parallel

Resistance of printed circuit board to the connector ≈ 0.2mΩ

Inductance of printed circuit board to the connector ≈ 0.2nH

$$R_{CONN} = \frac{20m\Omega}{11} + 0.2m\Omega = 2.02m\Omega$$

$$L_{CONN} = \frac{4.28nH}{11} + 0.2nH = 0.59nH$$

Step 2: Establish an allowable maximum voltage drop, ΔV_{OUT}, at the output.

Application Note U-156 [3] discusses the use of non-integrating gain which allows a larger voltage deviation during a load transient. Set the minimum load regulation to be V_{NOM} +3% ±1%. Therefore, a -7% voltage deviation is allowed on the output voltage while still meeting a minimum overall voltage of -5%. Voltage ripple is not considered during this transient response as the duty cycle is effectively 100%, and there is no voltage ripple. These limits are illustrated in Figure 6.

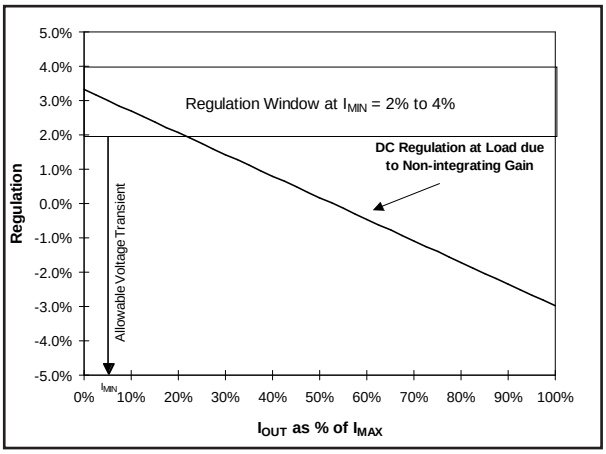

Figure 6. Setting the Regulation and Voltage Transient Requirements

$$\Delta V_{OUT} = 0.07 \bullet 3.1V = 0.217 \text{ volts}$$

Step 3: Estimate the total parasitic inductance, L_S, in order to derive a required value of R_S from the voltage step at the end of Phase 1. Aluminum electrolytic capacitors, size 10mm x 20mm, are estimated to have an ESL of approximately 4.0nH. Size 1206 ceramic chip capacitors are estimated to

have an ESL of approximately 1.9nH [1]. Assume that the combined ESL will be less than 0.51nH, for a total parasitic inductance

L_S = 1.10nH

This value must be insured to maintain overall regulation limits during the first phase, T_{STEP}.

Step 4: Equate the voltage deviation at the end of Phase 1 to the allowed voltage step. Assume that the change in voltage due to capacitive discharge is less than 1% of the overall change.

Therefore, the minimum value of C_{OUT} is equal to

$$C_{OUTmin} = \frac{10.9A \bullet 360ns}{2 \bullet 0.217V \bullet 0.01} = 904\mu F$$

Solving for the maximum value of R_S for a step of 11.2A – 0.3A = 10.9A yields,

$$R_S = \frac{(0.217V \bullet 0.99) - \left(10.9A \bullet \frac{1.1nH}{360ns}\right)}{10.9A}$$

$$= 16.6m\Omega$$

Step 5: Equate the voltage deviation at the end of Phase 2 to the allowed voltage step, from which a minimum value of C_{OUT} can be obtained

$$0.217V = \left(\frac{10.9A}{2}\right) \bullet \left(\frac{2 \bullet 5.0\mu s - 360ns}{C_{OUTmin}}\right) + (13.8m\Omega \bullet 10.9A)$$

$$C_{OUTmin} = \frac{\frac{10.9A}{2}(2.5\mu s \bullet 360ns)}{0.217V - (16.6m\Omega \bullet 10.9A)}$$

$$= 1457\mu F$$

Step 6: Choose a capacitor type, manufacturer(s) and values. Determine the number of capacitors required to meet the ESR requirements from Step 4 and the minimum capacitance requirements from Step 5. Add 20% margin for variations in ESR from 20°C down to 10°C (minimum operating temperature).

Radial, high frequency aluminum electrolytic capacitors are chosen based on the height allowed for this power supply VRM as well as their inherently low ESR and ESL. Many manufacturers offer 6.3V low ESR devices rated for 100kHz - 200kHz operation. Sanyo's MV-GX series of aluminum electrolytic capacitors are chosen based on their lower ESR specifications.

ESR Required = 16.6mΩ • 0.8 = 13.3mΩ

Sanyo MV-GX 1500µF, 10mm x 20mm, 6.3V device has a rated maximum ESR of 44mΩ. 4 devices are required, using 400mm^2 of board area. Sanyo MV-GX 1000µF, 8mm x 20mm, 6.3V device has a rated maximum ESR of 64mΩ. 6 devices are required, using 384mm^2 of board area. The 1500µF device is chosen to reduce the total parts count. The solution is:

C_{OUT} = 1500µF • 4 = 6000µF

ESR = 44mΩ / 4 = 11.0mΩ

ESL ≈ 4nH / 4 = 1.0nH

Step 7: Determine the voltage waveform at the output given this solution of output capacitors.

The current in the capacitor, during a transient, ramps up (or down) in a time determined by the output inductor. The output inductor, during a transient load step, is approximately 26µH.

$$T_{LOUT} = \left(\frac{I_{STEP}}{(V_{IN} - V_{OUT})}\right) \bullet L_{OUT}$$

$$= \left(\frac{10.9A}{(5.0V - 3.1V)}\right) \bullet 26\mu H = 149\mu s$$

The capacitor current is defined as

$$iC_{OUTt} = I_{STEP} - \frac{I_{STEP}}{T_{LOUT}} \bullet t$$

The voltage drop at the output of the power supply, during Phase 3 (T_{LOUT}) of the load transition, is determined by

$$\Delta V_{OUT} = \frac{I_{STEP}}{C_{OUT}} \bullet \left(t - \frac{T_{STEP}}{2} + T_{LOOP} - \frac{t^2}{2 \bullet T_{LOUT}}\right) + I_{STEP} \bullet \left(ESR - \frac{ESR \bullet t}{T_{LOUT}} + R_{CONN}\right)$$

The entire voltage response is plotted in Figure 7. Ceramic and tantalum capacitors (C11, C12, C29) are added in parallel to the aluminum output capacitors to reduce the overall ESL to less than the required

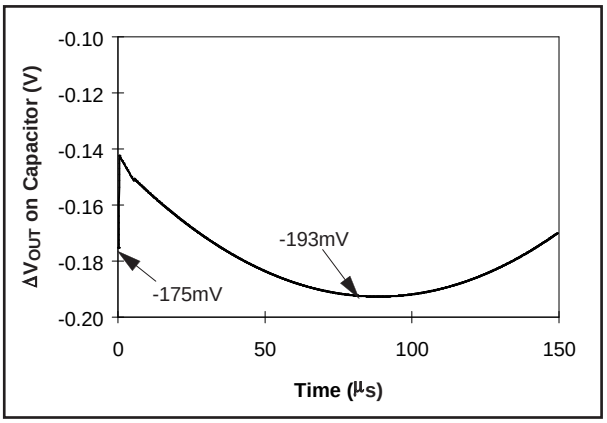

Figure 7. Voltage Droop on Power Supply Output during Load Transient

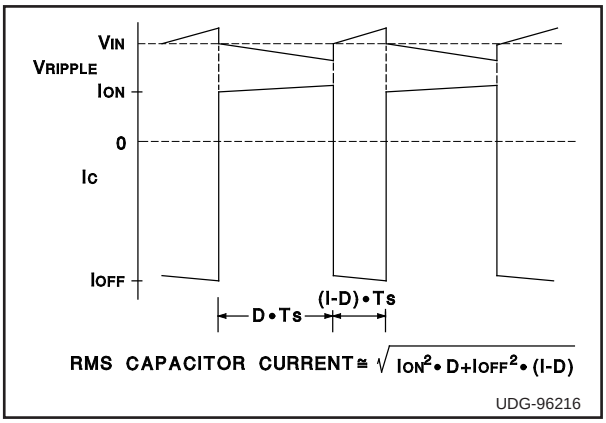

Figure 8. Input Capacitor(s) Current Waveform

0.51nH and to reduce high frequency noise to meet the ripple requirement of ≤2% peak-to-peak.

Input Capacitors: C01-C05

SANYO - 6MV1500GX - 3 in Parallel

C = 1500µF

Form Factor = 10 x 20mm, Radial

ESR = 0.044Ω

ESL ≈ 4nH (Estimated)

Ripple Current Rating = 1.25A @ 105°C, 100kHz

The input capacitance for a Buck regulator is chosen based on several criteria:

a) Ripple Current Handling at F_{SWITCH}
b) Ripple voltage at F_{SWITCH}
c) Maintaining Input voltage during load transients

The resulting solution must present a very low impedance to the input supply and to the Buck Regulator, resulting in a need for low ESR, large value capacitors.

Ripple Current and Voltage

The input capacitors are chosen primarily based on their switching frequency RMS current handling capability. With just 10's of nanohenries parasitic input inductance the input capacitors must handle virtually all of the 200kHz switching current.

Figure 8 shows the switching waveforms in the input capacitor(s). The average VRM power supply input current is calculated based on the maximum load of the power supply and the efficiency at maximum load.

$$I_{AVG} = \frac{P_{INPUTmax}}{V_{INPUT}} = \frac{I_{Omax} \bullet V_{OUT}}{Efficiency \bullet V_{INPUT}}$$

$$= \frac{11.2A \bullet 3.1V}{0.80 \bullet 5.0V} = 8.68A$$

During the MOSFET ON time, the input capacitors must provide the difference between the load current and the input current. During the MOSFET OFF time, the capacitor current is the complete input average current. Therefore,

$$I_{ON} = I_{Omax} - I_{AVG} = 11.2A - 8.68A = 2.52A$$
$$I_{OFF} = -I_{AVG} = -8.68A$$

The duty cycle at the maximum operating current is approximately 73%, and therefore the RMS current in the capacitors, assuming a rectangular waveform since the current ramp is very small, is given by

$$I_{RMS} = \sqrt{I_{OFF}^2 \bullet (1 - Duty) + I_{ON}^2 \bullet Duty}$$
$$= 5.0\ A_{RMS}$$

Three (3) Sanyo capacitors are chosen to maintain reliable operation while operating at this RMS current level.

Given the current waveform of Figure 8, the input voltage ripple will be proportional to the input capacitance and ESR, as shown in the voltage waveform of Figure 8. Low ESR and high capacitance will keep the ripple voltage low.

C01 and C02 ceramic capacitors are added to filter high frequency noise from the switching power supply from the +5V input power bus.

Filtering V_{INPUT} During Load Transients

During a low-to-high output load transient, the duty cycle goes to 100% until the output inductor current is equal to the load current, and the output inductor limits di/dt of the input current. During a high-to-low output load transient, however, there is no output

inductor limiting the input current rate because the input switch is opened (0% duty cycle). The result is the +5V bulk power supply will continue to source high current into this power supply for some time. Figure 9 illustrates the difference in the circuits between a low-to-high and a high-to-low load transient.

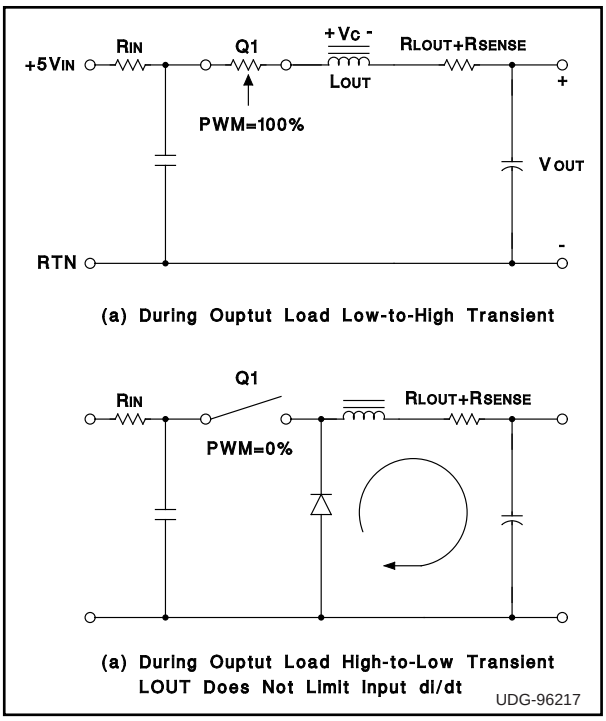

Figure 9. Lout limits the input current only on a low-to-high output current transient

Figure 10 shows typical current waveforms during a high-to-low load transient. The output current abruptly stops but the +5V bulk power supply takes a finite time to react to this change in load current, therefore sourcing energy into the input capacitors. Intel specifies that this input current must not change at a rate faster than 0.1A/µs.

The input capacitor(s) are chosen to limit the voltage surge on the input capacitors to less then 0.15 volts (3% of V_{IN}) during a high-to-low load transient. The current in the capacitor(s) is defined as

$$iC_{IN(t)} = I_{AVG} - I_{In\_Rate} \bullet t$$
$$= 8.68A - (0.1A/\mu s) \bullet t$$

where I_{In_Rate} is defined as the rate at which the input current decays based on the +5V bulk power supply, assumed here to be 0.1A/µs, therefore decaying to 0.0A in 86.8µs.

The voltage surge on the input capacitance during this time is

$$vC_{IN(t)} = \frac{1}{C_{IN}} \int_0^{86.8\mu s} = iC_{IN(t)} + (ESR_{IN} \bullet iC_{IN(t)}) =$$

$$\left(\frac{8.68}{Cin} - (10^5 \bullet ESR)\right) \bullet t - \left(\frac{10^5 \bullet t^2}{2 \bullet C_{IN}}\right) + 8.68 \bullet ESR$$

which is plotted in Figure 11 for 3 Sanyo MV-GX type 1500µF, 0.044Ω Aluminum Electrolytic Capacitors.

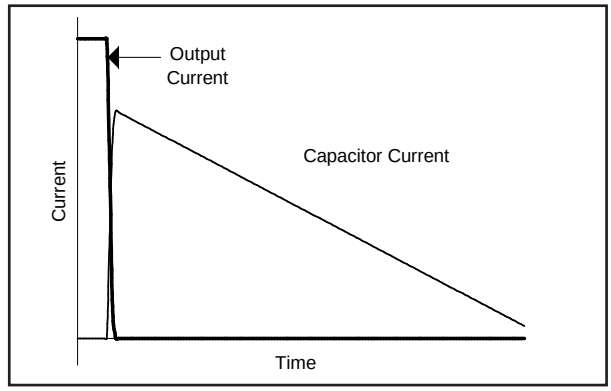

Figure 10. Current Waveforms during High-to-Low Output Transient

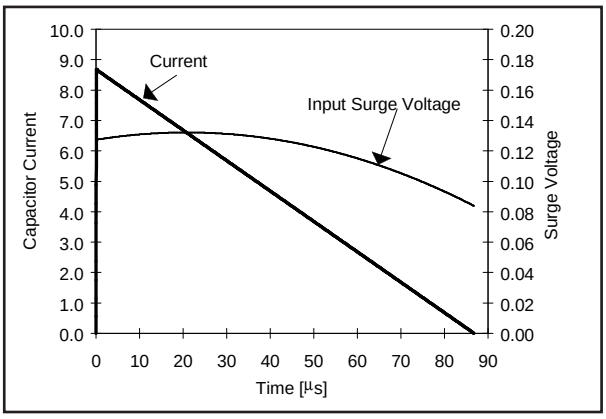

Figure 11. Input Capacitor Current and Surge Voltage During a High-to-Low Load Transient

Sense Resistor: R01

Dale P/N WSR-2 0.01Ω 1%

10mΩ, 2.0 watt 2 wire SMD sense resistor, ±75ppm TCR

The sense resistor is chosen by the criteria discussed in U-156, Appendix 5 [3]. R_{SENSE} is a 2-wire, 2 watt surface mount power product with very low inductance. The 2 watt rating (to ambient temperatures of 75°C) allows for 50% derating at the typical maximum current of 9.9 Amperes [1].

A short circuit current, I_{SC}, is chosen at a nominal 12.5 Amperes, more than 10% over the maximum current. The value of the UC3886 Current Amplifier's gain, G_{CSA}, is bounded to

$$G_{CSA\_MIN} = 5.0 \text{ and } G_{CSA\_MAX}$$
$$= 2.5MHz/200kHz$$

From

$$G_{CSA} \bullet R_{SENSE} = \frac{1.0\ Volt}{I_{SC}}$$

A 12.5A limit implies that Rsense must lie between 0.0064Ω and 0.016Ω. Choose 0.010Ω as the lowest standard value.

The power dissipation in R_{SENSE} during normal and short circuit conditions is

Normal:

$$P_D = I_{AVG}^2 \bullet R_{SENSE} = 9.9^2 \bullet 0.010\Omega$$
$$= 0.98\ Watt = 49\%\ of\ rated$$

Short Circuit:

$$P_D = I_{SC}^2 \bullet R_{SENSE} = 12.5^2 \bullet 0.010\Omega$$
$$= 1.56\ Watt = 78\%\ of\ rated$$

CONFIGURING THE UC3910 4-BIT DAC AND VOLTAGE MONITOR AND THE UC3886 AVERAGE CURRENT MODE PWM CONTROLLER

With the power stage chosen, the UC3910 and UC3886 are ready to be programmed for the proper operation. Figure 12 and Figure 13 show block diagrams for the UC3886 and the UC3910 ICs.

Grounding

The UC3886 signal ground (SGND) pin as well as the UC3910's two ground pins are referenced to the output voltage return path for best regulation and noise immunity. The PGND pin of the UC3886 is referenced to the input voltage return path, as discussed in U-156 [4], for best gate drive performance.

Decoupling

High frequency decoupling is provided at the VCC power pins (C14, C18) and the VREF pins (C13, C17) of both ICs. VCC is decoupled to PGND on the UC3886 additionally with a low ESR 0.1µF capacitor (C19) to provide a low impedance gate drive source.

Set the UC3886 Oscillator Frequency to 200kHz

During a load transient, a very high duty cycle is desired. Therefore, set the maximum duty cycle to 99%. From the UC3886 Data Sheet:

$$D_{MAX} = 1 - \frac{2.0V}{(R_T \bullet 4.0mA)} = 0.99 \rightarrow$$

$$R_T = \frac{2.0V}{(1 - D_{MAX}) \bullet 4.0mA} = 50k\Omega$$

$$C_T = \frac{2.0V \bullet ((4.0mA \bullet R_T) - 2.0V]}{F_S \bullet 1.8V \bullet R_T^2 \bullet 4.0mA} = 110pF$$

Choose C_T = 100pF (C20)
R_T = 54.9kΩ (R10)

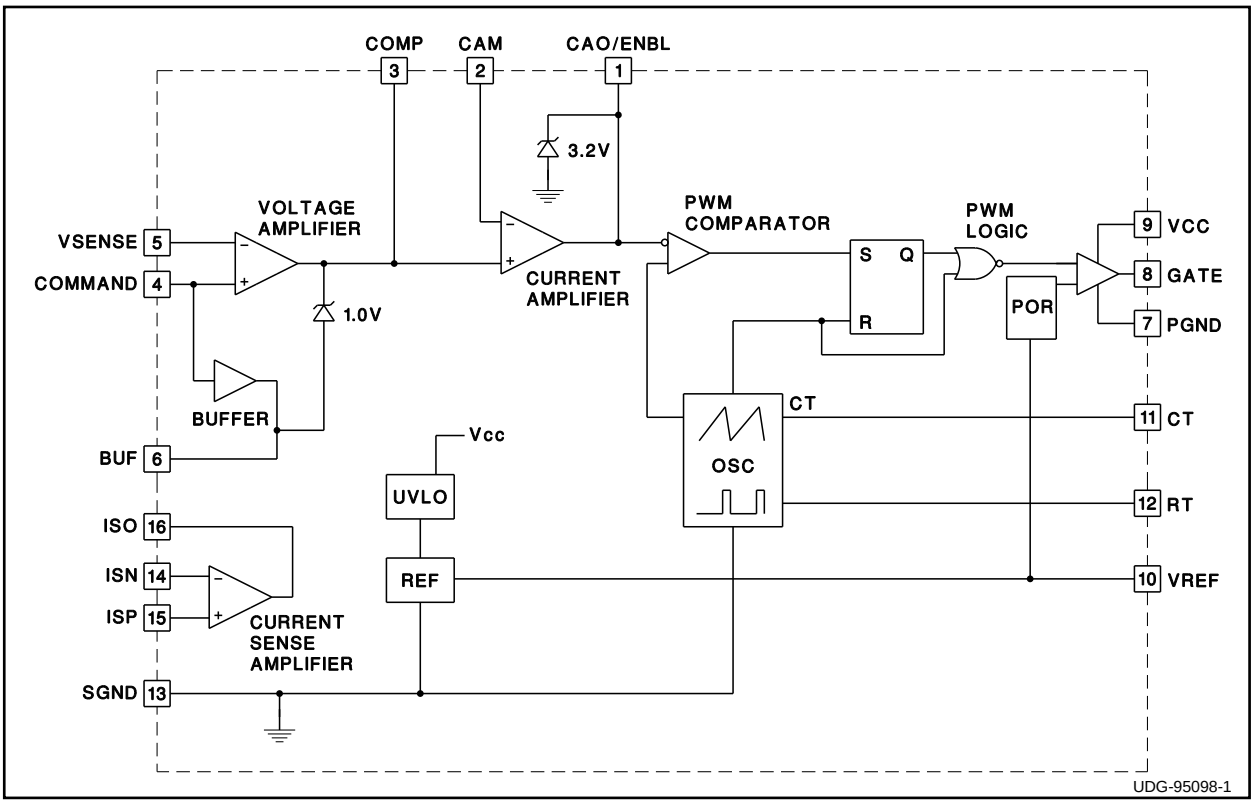

Figure 12. UC3886 Average Current Mode PWM Control IC

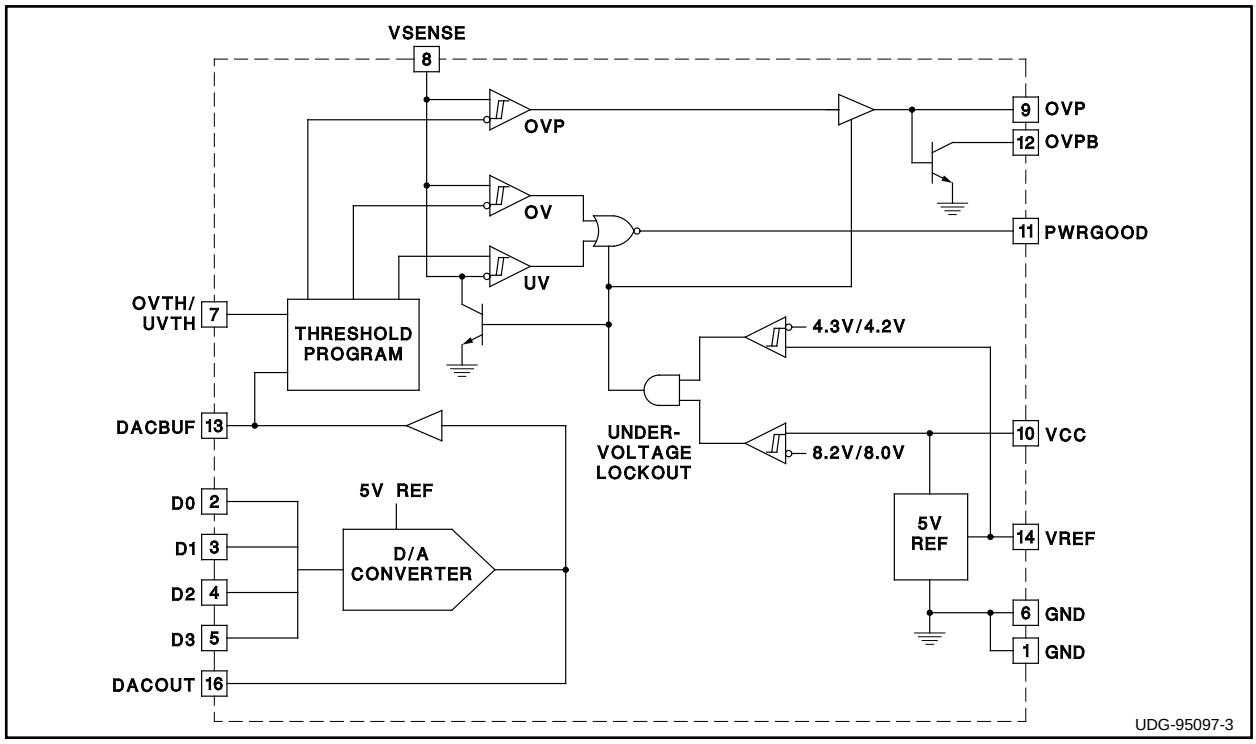

Figure 13. UC3910 4-BIT DAC and Voltage Monitor IC

Note that internal capacitance on the UC3886 CT pin adds approximately 10 to 15pF of capacitance. When using a capacitor as low as 100pF, a substantial frequency shift can result.

A 24Ω resistor and Test Point 1 (R11 and TP1) are provided to allow external synchronization of the unit from a narrow synchronizing pulse [3]. This resistor is not required unless external synchronization is desired.

Driving the MOSFET Gate from the UC3886 Gate Drive Output

A 10Ω gate drive resistor (R12) is placed close to the MOSFET gate. The 10Ω resistor limits the peak current and provides damping at the MOSFET gate to prevent oscillations. The power dissipation in this resistor is approximately 1.0mW based on an average current of 10mA.

Figure 14 shows that the current path for a gate drive signal originates from C19, a low decoupling capacitor located closely to the UC3886 GATE pin. C10 is added from the input voltage to the Power Ground (PGND) to decouple the high frequency current spike which exits the MOSFET from the DRAIN and must find a path back to PGND. C10 should be located as closely as possible to the MOSFET to prevent high frequency ringing at the MOSFET.

U3, the UC3612 dual schottky diode, is added to protect the UC3886 from inductive spikes above V_{CC} and below ground which may occur due to high gate drive spikes and parasitic inductance.

External Enable Signal

Intel specifies [1] that the Pentium®Pro power supply be enabled by an open collector, active high signal, OUTEN.

The UC3886 CAO/ENBL is connected to the input of the UC3886 PWM comparator (Figure 12), with the other side of the comparator attached to the oscillator ramp. The oscillator ramp is nominally a 1.0V to 2.8V peak ramp signal. The UC3886 gate drive is disabled by bringing the CAO/ENBL signal to a level below the oscillator ramp signal.

The external OUTEN signal is connected to the UC3886 CAO/ENBL signal through a 1.0kΩ resistor, R2. A 1.0kΩ resistor is recommended to provide a high impedance buffer between external noise and the output of the UC3886 Current Amplifier Output, to insure noise does not couple into the control loop. The CAO/ENBL pin may source up to 400µA. Using a 1.0kΩ resistor will result in a 400mV drop. A reasonable open collector output stage will be able to sink 400µA and maintain a saturation voltage less than 400mV, keeping the LOW level voltage at CAO/ENBL to less than 800mV.

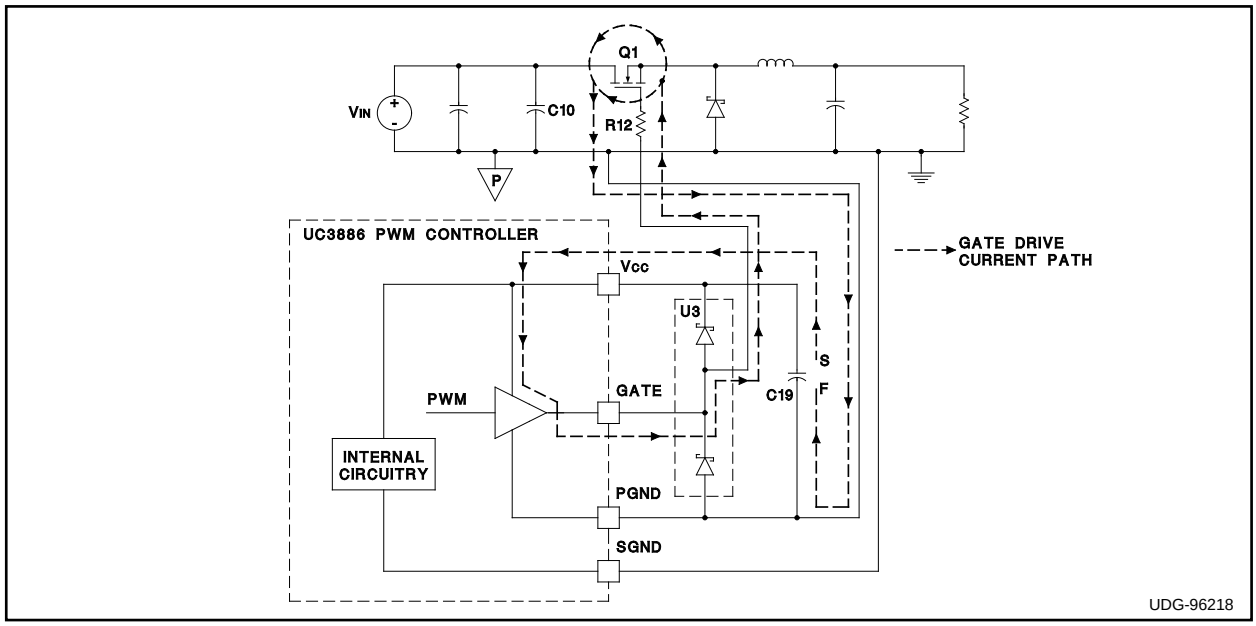

Figure 14. Driving Q1 with the UC3886

External Signal UP#

Intel specifies [1] that the UP# signal be used to disable the power supply if it is not capable of supporting an upgraded processor, either by varying the voltage or by supporting the higher load currents. The UP# signal is also an open collector signal, normally high, but pulled low when an Upgrade Processor is in place. By inserting a 0Ω jumper resistor for R25, the power supply will be disabled in the case of an upgrade processor.

> THE UNITRODE DEMONSTRATION KIT IS SHIPPED WITHOUT R25. UPGRADE PROCESSORS MAY EXCEED THE 12.5A CURRENT LIMIT OF THE DEMONSTRATION KIT. INSERT A 0Ω 0603 SMD JUMPER RESISTOR FOR R25 TO DISABLE THE POWER SUPPLY IN AN UPGRADE PROCESSOR APPLICATION

CONFIGURING THE UC3910 VOLTAGE MONITORING AND PROTECTION FEATURES

The regulation requirements for this power supply are set at ±5%. The PWRGD requirement is set to signal a voltage regulation failure when the output voltage is outside of the range of ±10%. The UC3910 Undervoltage and Overvoltage (UV, OV) thresholds are therefore chosen at midrange to be nominally ±7.5%.

The equations for setting the Voltage Monitoring thresholds (see U-158 [7]) are

$$\%V_{UV} = -\left(R_{DIV} \bullet \frac{3.34k\Omega}{20k\Omega}\right) \bullet 100 = -(R_{DIV} \bullet 16.7)$$

$$\%Vov = R_{DIV} \bullet 16.7$$

$$\%Vovp = R_{DIV} \bullet 33.4 = \%Vov \bullet 2.0$$

Setting $\%V_{UV}$ and $\%V_{OV}$ to ±7.55 yields a divider ratio R_{DIV} of 0.45.

R8 and R9 act as a voltage divider between the UC3910's DACBUF pin and OVTH/UVTH pin. R8 and R9 are chosen to draw approximately 1.0mA.

R8 = 1.69kΩ , R9 = 1.34kΩ, R_{DIV} = 0.448

The nominal thresholds are

Overvoltage Threshold	= +7.48%
Undervoltage Threshold	= –7.48%
Overvoltage Protection Threshold	= +14.96%

PWRGD Signal:

Intel requires [1] the PWRGD signal to be an open collector active HIGH signal when the voltage is within specification. R7 is a 4.7kΩ resistor which can be added internally to the demonstration kit power supply for evaluation purposes. See the schematic of Figure 2.

> R7 IS NOT INSTALLED ON UNITRODE'S DEMONSTRATION KIT. USE A 4.7kΩ 1/10W 0603 SMD RESISTOR IF INTERNAL PULLUP IS DESIRED.

Overvoltage Protection:

The UC3910 provides both OVP and OVPB pins for protection in the case of overvoltage. OVP is capable of driving an SCR to perform a crowbar func-

tion. OVPB is an open collector, active low signal which is designed to pull down on the UC3886 CAO/ENBL signal to disable the UC3886 gate drive.

The Overvoltage Protection circuit consists of F1, SCR1, CR2, R05 and R06. Fuse F1 serves to protect the circuit under two circumstances: a MOSFET short circuit failure and when the crowbar SCR is fired. The fuse is chosen based on the maximum operating power and efficiency.

$$P_{OUTmax} = 3.4 \text{ Volts} \bullet 11.2 \text{ Amps} = 38 \text{ Watts}$$

$$I_{INmax} = \frac{38 \text{ Watts}}{0.80 \bullet 5.0V} = 9.5 \text{ Amperes}$$

A 10 Ampere SMD fuse is chosen.

Characterizing SCR's for Crowbar Applications is discussed extensively in Motorola's Thyristor Device Data book [5]. SCR1 is chosen based on its low gate trigger current, its On-State RMS current rating, and because it has to discharge a substantial amount of low ESR aluminum capacitors, its Peak Non-repetitive surge current rating.

SCR1 by itself will not protect the Pentium®Pro processor against an overvoltage except by causing the fuse F1 to open, which can take a substantial amount of time. CR2 provides an additional path to discharge the output capacitors directly in order to clamp the output voltage and protect the processor immediately. CR2 is connected before the sense resistor, R1, in order to use R1 as a current limiting resistor when the crowbar is fired. CR2 has a rated surge current of 200 Amperes.

Connecting an SCR as a crowbar to the output voltage may appear to be the best way to protect the Pentium®Pro processor in the case of an overvoltage failure. However, the UC3886 provides a current limiting mechanism, which would cause the SCR to sink the programmed current limit. An input fuse would not open under these circumstances because of the low output power being delivered. The SCR on the output would most likely fail thermally and open, thus defeating the protection mechanism.

Resistor R6 from the SCR gate to ground is chosen to protect the SCR against false firing due to dv/dt conditions. R6 will draw approximately 15mA when the SCR is fired, as the gate voltage is approximately 1.5 volts. R5 is chosen to limit the current from the UC3910 while insuring that the SCR gate trigger current is sufficient down to 10°C. The UC3910 will source at least 65mA when activated. R5 limits the current preventing excessive droop on VCC when the SCR is fired.

The open collector signal OVPB is also triggered during an overvoltage protection fault. This signal can be used to disable the UC3886 gate drive by connecting it directly to the UC3886 CAO/ENBL signal. R26 is installed in Unitrode's demonstration kit as a “jumper” only, to enable or disable this feature. Normal applications will directly connect the UC3886 CAO/ENBL pin to the UC3910 OVPB pin. Note that the OVPB signal is an open collector signal and therefore may be “OR';d” with the external open collector OUTEN and UP# signals.

Setting the RC Filters at VSENSE and DACOUT of the UC3910

The UC3910 VSENSE pin requires an R-C filter to isolate the pin from the power supply output [6]. The resistor acts both as part of an R-C filter and to limit the current into the VSENSE pin. During UVLO of the UC3910, VSENSE is actively pulled low in order to prevent false overvoltage protection signals.

The filter resistor R3 is chosen to limit the input current to ≤500µA under the maximum programmable voltage for the Pentium®Pro.

$$R3 \quad \frac{3.4V}{500\mu A} = 6.8k\Omega$$

The filter capacitor C16 is chosen to set the filter corner frequency at approximately $F_{SWITCH}/10$ in order to reduce the switching frequency ripple by 20dB.

$$C16 = \frac{1}{R3 \bullet 2 \bullet \pi \bullet (200kHz/10)} = 1170pF$$

Use R3 = 6.8kΩ

C16 = 1200pF as standard values

The filter capacitor at the output of DACOUT, C15, is chosen to insure that DACOUT rises at a faster rate than VSENSE. This prevents false OVP signals during V_{CC} brownout or glitch conditions.

$$R3 \bullet C16 > 3k\Omega \bullet C15 \rightarrow$$

$$C15 \leq \frac{R3 \bullet C16}{3k\Omega} \quad 2720pF$$

Use C15 = 2700pF as a standard value

Note that resistor R4 connected to the UC3910 VSENSE pin is used for debug purposes only and is not required for normal operation.

Programming the Current Limit with the Current Sense Amplifier of the UC3886

A nominal current limit of 12.5 Amperes is desired to protect the power supply under short circuit con-

ditions. Accurate current limiting is advantageous in this Buck regulator as it limits the power dissipated in the freewheeling diode under short circuit conditions.

The gain of the current sense amplifier, G_{CSA}, is set based on the desired current limit and the value of the sense resistor [4], using:

$$G_{CSA} \bullet R_{SENSE} = \frac{1.0\ Volt}{I_{SC}} \rightarrow$$

$$G_{CSA} = \frac{1.0\ Volt}{12.5A \bullet 0.01\Omega} = 8.0$$

The current sense amplifier is configured as a differential amplifier using four external resistors, R18, R19, R20 and R21, with the gain equal to

$$G_{CSA} = 8.0 = \frac{R20}{R18} = \frac{R21}{R19}$$

R20 and R21 should not load down the UC3886 Current Sense Amplifier, and are chosen as 33.2kΩ. Therefore

Use R20 = R21 = 33.2kΩ
R18 = R19 = 4.22kΩ resulting in
G_{CSA} = 7.87 and a nominal short circuit current limit, I_{SC}, of 12.7 Amperes.

The BUF signal at pin 6 of the UC3886 must be filtered by C22 to insure a noise free bias voltage for the current sense signal ISO.

Programming the Non-Integrating Gain for the Voltage Amplifier of the UC3886

Managing the voltage regulation at the load, and maintaining regulation of ±5% involves the use of non-integrating gain about the UC3886 voltage amplifier. Without non-integrating gain, the number of output capacitors must increase. Application note U-156 [4], Appendix 3, details the goals and requirements for programming non-integrating gain.

The specified regulation window is ±5%. V_{RIPPLE} and DC Error, which are each ±1%, reserve ±2% of the specified window. This leaves ±3% of the window for load regulation. The desired regulation performance, versus load current, is shown in Figure 15. Setting the low load regulation to +3% nominally will allow the maximum voltage excursion during a load transient.

The UC3886 error voltage, COMP, will vary with load current from 0.0A to I_{SC} = 12.7A. The change in the error voltage will be

$$\Delta Ve = \frac{I_{MAX}}{I_{SC}} \bullet 0.95V = \frac{11.2\ Amps}{12.7\ Amps} \bullet 0.95V$$
$$= 0.834\ Volts$$

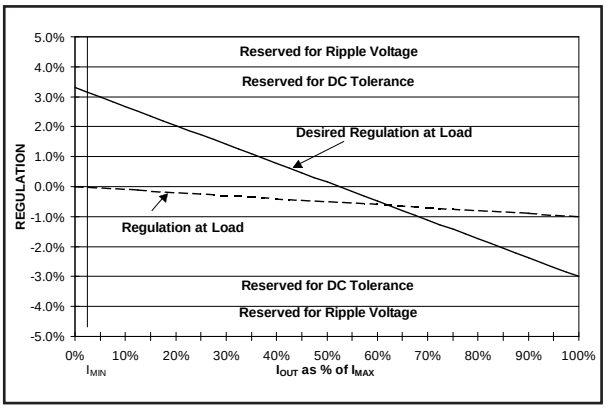

Figure 15. Load Regulation

A change in COMP of 0.95 volts is used because the change is 1.0V ±50mV, and under worst case the regulation window must be held.

Figure 15 shows that the load regulation due to parasitic resistances is –1% from no load to maximum load. From the desired load regulation curve, the swing in output voltage associated with the change from 0 Amps (Not I_{MIN} in this case) to I_{MAX} is determined to be –6.3%. The I • R drop intrinsic to the circuit is then subtracted and the desired regulation swing is set at –5.3%. From the lowest operating voltage, the change in the output voltage is

$$\Delta V_{OUT} = 2.4\ V \bullet 5.3\% = 0.127\ Volts$$

The gain around the Voltage Amplifier determined by the ratio of R16 to R14 is chosen to achieve the desired voltage swing over the operating load range.

$$\Delta V_{OUT} = \frac{\Delta V_E}{Gain} = \frac{\Delta V_E}{R16/R14} \text{ and}$$

$$\text{therefore } R16/R14 = \frac{0.88V}{0.127V} = 6.57$$

The feedback resistor is chosen very large to insure that there are no loading effects on the voltage amplifier output.

Use R16 = 100kΩ
R14 = 15kΩ resulting in the gain about the Voltage Amplifier of 6.67.

Non-Integrating gain has a negative regulation slope with regards to load current, and must be shifted up in order to swing ±3% about the nominal voltage. A DC offset is created by the resistive divider of R14 and R17 which shifts the regulation window up by +3.1%. R17 is chosen by

$$(V_{NOM} + 3\%) \bullet \frac{R17}{R14 + R17} = V_{NOM}$$

and therefore

$$\frac{R17}{R14 + R17} = \frac{1}{1.03}$$ yielding R17 = 487kΩ.

Filtering and Canceling Offset Current at the Command Pin of the UC3886

It is recommended that the decoupling capacitor, C21 be placed very close to the COMMAND pin of the UC3886, as this voltage is the voltage which commands the power supply output, and noise will directly couple to the power supply output. R13 is added in series between the UC3910 DACOUT pin and the UC3886 COMMAND pin in order to minimize DC errors due to offset currents in the UC3886 voltage amplifier. R13 is chosen to match the impedance at the V_{SENSE} input to the UC3886 voltage amplifier. Remember that the UC3910 DACOUT pin has an internal 3kΩ resistor. Therefore

$$R13 = \frac{1}{\frac{1}{R16} + \frac{1}{R14} + \frac{1}{R17}} - R_{DAC} =$$

$$= \frac{1}{\frac{1}{100k\Omega} + \frac{1}{15k\Omega} + \frac{1}{487k\Omega}} - 3k\Omega = 9.7k\Omega$$

Use R13 = 10kΩ

CLOSING THE LOOP WITH THE UC3886 AVERAGE CURRENT MODE PWM CONTROLLER

The basis for closing the Average Current and the Voltage loops of this circuit is found in Unitrode Application Note U-140 [2] and in the Unitrode Seminar Topic “Switching Power Supply Control Loop Design” [7]. This application note presents a step-by-step methodology solving for the loop compensation components found in Figure 2. The current loop is completed first with the voltage loop to follow.

The goal in closing the loops for this power supply is to obtain a stable closed loop response for the current and voltage loops, with an overall closed loop crossover frequency between 10kHz and

$$\frac{F_S}{2\pi} = 32kHz.$$

Closing the Current Loop

Step 1: Calculate the Oscillator Ramp as seen at the PWM Comparator input. From U-140, it is known that “The amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input”.

From the oscillator timing equations, the ramp slope is

$$T_S = \frac{1}{F_S} = 5.0\mu s$$

$T_D \approx 50ns$ (Deadtime of oscillator)

Ramp = 2.8V – 1.0V = 1.8Vp-p

$$\text{Ramp Slope} = \frac{\text{Ramp}}{T_S - T_D} = \frac{1.8V}{4.95\mu s}$$

= 0.364 Volts/µs

Step 2: Calculate the inductor current downslope. The downslope occurs during the Buck regulator switch OFF time.

The inductor downslope is maximum at the maximum output voltage and with the minimum output inductance, which occurs at maximum load and maximum output voltage.

The diode forward voltage of CR1 is approximately 0.35V at 11.2A

V_{OUTmax} = 3.4V

L_{OUT} at the maximum operating current = 12µH

$$\text{Inductor di/dt} = \frac{3.4V + 0.35V}{12.0\mu H} = 0.313A/\mu s$$

Step 3: Convert the inductor current downslope to a voltage downslope as seen at the output of the Current Sense Amplifier.

Inductor dv/dt = 0.313A/µs • 0.01Ω •

$$\frac{33.2k\Omega}{4.22k\Omega} = 24.6mV/\mu s$$

Step 4: Set the gain from the Current Amplifier to meet the slope criteria. Reduce G_{CAmax} by 25% to account for amplified voltage ripple due to the ESR of the output capacitors. Reduce the gain by 15% more to account for Inductor and Oscillator variations.

The oscillator Ramp Slope = 0.364V/µs ≥ G_{CA} • Inductor dv/dt

where G_{CA} = The gain of the Current Amplifier at the switching frequency

Therefore:

$$G_{CA} \text{ at } F_{SWITCH} = \frac{364mV/ms}{24.6mV/ms} \bullet 0.60 = 8.9$$

Resistors R23 and R24 set the inverting

gain about the UC3886 Current Amplifier. Pick R24 to limit the loading on the Current Amplifier output. Then set R23 and R24 to program the Current Amplifier's inverting gain at F_{SWITCH}.

Use

R24 = 10.5kΩ

R23 = 1.24kΩ

as standard values

G_{CA} = 8.47

The GBW product for the UC3886 Current Amplifier is 3.5MHz and therefore a gain of 8.47 at 200kHz is within the device's GBW.

Step 5: Find the crossover frequency of the current loop gain by first finding the small signal control-to-output gain, G_P, of the buck regulator current loop power section. Consider the fact that the inductor, L_{OUT}, plays a key role in the equation for G_P, and that since L_{OUT} swings significantly with load current, so does G_P.

The small signal control-to-output gain is defined in U-140 from the CA output, V_{CA}, to the voltage across the sense resistor, V_{RS}. The UC3886 application however must add a gain stage factor for the Current Sense Amplifier gain. G_P is determined by

$$\frac{V_{RS}}{V_{CA}} = \left(\frac{Duty}{V_{CA}}\right) \bullet \left(\frac{V_{RS}}{I_{Lout}}\right) \bullet \left(\frac{I_{Lout}}{Duty}\right) \bullet G_{CSA}$$

$$= G_P$$

The change in duty cycle to change in Current Amplifier output is 100%/V_S, or

$$\frac{Duty}{V_{CA}} = \frac{1}{V_S}$$

where

V_S = The peak-to-peak voltage change of the oscillator ramp

The change in the resistor voltage to change in the inductor current is simply the value of the sense resistor, R_S (R_S = R1 in Figure 2).

$$\frac{V_{RS}}{I_{Lout}} = Rs$$

The change in inductor current per the change in duty cycle is a function of the input voltage. The small signal voltage applied at the inductor is simply the small signal changes in V_{IN} • Duty. The change in inductor current per the change in applied inductor voltage (small signal) is given by:

$$\frac{i}{v} = \frac{1}{Z_{OUT}} \text{ where } v = V_{IN} \bullet Duty$$

and therefore $$\frac{I_{Lout}}{Duty \bullet V_{IN}} = \frac{1}{Z_{OUT}}$$

which leads to the transfer function of

$$\frac{I_{Lout}}{Duty} = \frac{V_{IN}}{Z_{OUT}}$$

Z_{OUT} is dominated by the output inductor at frequencies above the L • C resonant frequency, and results in a single pole rolloff due to that inductor, which is what is shown in U-140 as the "$V_{IN/S}$ • L_{OUT}" term. The complete impedance function includes the output Inductor, Capacitor, Sense Resistor, Inductor Resistance, ESR, ESL and Load Resistance. The parasitic resistances will help dampen the response at the resonant frequency and should not be ignored.

The output impedance is given by:

$$Z_{OUT} = s \bullet L_{OUT} + R_S + RLout + \frac{\left(\frac{1}{s \bullet C} + ESR + s \bullet ESL\right) \bullet RL}{\left(\frac{1}{s \bullet C} + ESR + s \bullet ESL\right) + RL}$$

where

R_{Lout} = DC Resistance of output inductor

C = Output capacitance

ESR = Output capacitance ESR

ESL = Output capacitance ESL

R_L = Load Resistance

Now, solving for the control-to-output gain, G_P (of the Current Loop only),

$$G_p = \left(\frac{Duty}{V_{CA}}\right) \bullet \left(\frac{V_{RS}}{I_{Lout}}\right) \bullet \left(\frac{I_{Lout}}{Duty}\right) \bullet GCSA$$

can be simplified as

$$G_P = \left(\frac{1}{V_A}\right) \bullet (R_{SENSE}) \bullet \left(\frac{V_{IN}}{Z_{OUT}}\right) \bullet G_{CSA}$$

U-140 states to multiply the control-to-output power loop gain, Gp, by the gain of the Current Amplifier to achieve the overall current loop gain.

$$\text{Loop} = G_P \bullet G_{CA} = \left[\left(\frac{1}{V_S}\right) \bullet \left(\frac{V_{IN}}{Z_{OUT}}\right) \bullet (R_S) \bullet G_{CSA}\right] \bullet \left[\frac{V_S \bullet L_{OUT}}{(T_S - T_D) \bullet R_S \bullet (V_O + V_F) \bullet G_{CSA}}\right]$$

Equating the current loop gain to 1 will yield the loop crossover frequency, F_C.

$$1 = \left[\left(\frac{1}{V_S}\right) \bullet \left(\frac{V_{IN}}{Z(2 \bullet \pi \bullet F_C)}\right) \bullet (R_S) \bullet G_{CSA}\right] \bullet \left[\frac{V_S \bullet L_{OUT}}{(T_S - T_D) \bullet R \bullet (V_O + V_F) \bullet G_{CSA}}\right]$$

Z_{OUT} is dominated by the output inductor in the region of the crossover frequency, and therefore $Z_{OUT(fc)}$ can be replaced by $s \bullet L_{OUT}$

Solving for F_C and simplifying yields:

$$F_C = \frac{V_{IN}}{2 \bullet \pi \bullet (V_O + V_F) \bullet (T_S - T_D)}$$

Notice that L_{OUT} falls out of the equation, and therefore the only “Load” dependency is in the value of Vf. This is true ONLY if Lout is Constant with load current. If a swinging choke is used, then Lout cannot drop out of the equation.

The crossover frequency of the current loop can therefore be determined by

$$\frac{V_{IN} \bullet R_S}{V_S \bullet 2 \bullet \pi \bullet F_C \bullet L_{OUT}} \bullet G_{CSA} \bullet G_{CA} = 1$$

and therefore

$$F_C = \frac{V_{IN} \bullet R_S}{V_S \bullet 2 \bullet \pi \bullet L_{OUT}} \bullet G_{CSA} \bullet G_{CA}$$

The crossover frequency of the current loop will therefore vary as a function of load, with the minimum crossover frequency at the maximum input voltage and maximum value of L_{OUT}, or at minimum load.

Solving for the crossover frequency:

$$F_{Cmax} = \frac{V_{Imax} \bullet R_S}{V_S \bullet 2 \bullet \pi \bullet L_{OUTmin}} \bullet G_{CSA} \bullet G_{CA}$$

$$= \frac{5.25V \bullet 0.01\Omega}{1.8V \bullet 2 \bullet \pi \bullet 120mH} \bullet 7.87 \bullet 8.47$$

$$= 25\ .8kHz$$

$$F_{Cmin} = \frac{V_{Imin} \bullet R_S}{V_S \bullet 2 \bullet \pi \bullet L_{OUTmax}} \bullet G_{CSA} \bullet G_{CA}$$

$$= \frac{4.75V \bullet 0.01\Omega}{1.8V \bullet 2 \bullet \pi \bullet 24.0\mu H} \bullet 7.87 \bullet 8.47$$

$$= 11.7kHz$$

where the input voltage is +5V ±5%

Step 6: Add the pole-zero compensation into the Current Amplifier by solving for C_{ZERO} (C25 + C28) and C_{POLE} (C27), and solve for the current loop transfer function.

The zero should be placed at or below the minimum current loop crossover frequency, F_{Cmin}. The value of C_{ZERO} is determined by

$$Czero = \frac{1}{2 \bullet \pi \bullet F_{Cmin} \bullet R24}$$

$$= \frac{1}{2 \bullet \pi \bullet 11.7kHz \bullet 10.5k\Omega}$$

$$= 1296pF$$

Use C_{ZERO} = C25 + C28 = 1220pF (2 capacitors are used to allow tuning of this frequency)

The pole should be placed at $F_S/2$. The value of C_{POLE} is determined by

$$C_{POLE} = \frac{C_{ZERO}}{(2 \bullet \pi \bullet F_S/2 \bullet R24 \bullet C_{ZERO}) - 1}$$

$$= \frac{1220pF}{(2 \bullet \pi \bullet = 200kHz/2 \bullet 10.5k\Omega \bullet 1220pF) - 1}$$

$$= 173pF$$

Use C_{POLE} = C27 = 180pF

The transfer function of the compensated current amplifier is

$$G_{CAs} = \frac{R24 \bullet (C_{POLE} + C_{ZERO}) \bullet s + 1}{s \bullet (C_{ZERO} \bullet R23 \bullet (R24 \bullet s \bullet C_{POLE} + 1)}$$

and the overall current loop is determined by multiplying the control-to-output transfer function by the current amplifier transfer function, or

$$Loop = G_P \bullet G_{CAs} = \left(\frac{1}{V_S} \bullet \frac{V_{IN}}{Z_{OUTs}} \bullet R_S \bullet G_{CSA} \right) \bullet G_{CAs}$$

which is plotted in Figure 16.

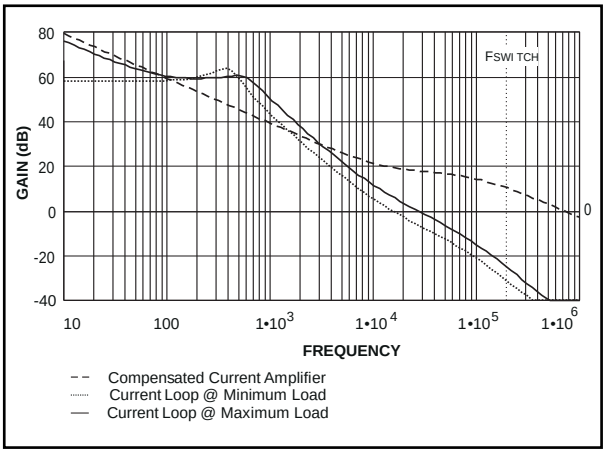

Figure 16. Current Amplifier and Current Loop Bode Plot - Minimum and Maximum Loads

The lower crossover frequency is above the estimated range of 11.7kHz because the gain of the compensated Current Amplifier is not a flat gain of 8.47 but is slightly higher due to the integrating feedback of the Current Amplifier.

The changes in loop gain at low frequencies is dominated by the changes in load resistance, while the variation at and around the crossover frequency is a function of the change in inductance vs current.

Closing the Voltage Loop:

The voltage loop must now be closed according to the guidelines in Unitrode Seminar Topic [7] "Switching Power Supply Control Loop Design". The compensation around the voltage amplifier of this circuit will differ from the seminar topic however by utilizing non-integrating gain [4].

Step 7: Generate a model for the closed current loop transconductance.

The small signal current loop can be modeled as a fixed gain at low frequencies equal the transconductance forced by the current loop, and having a pole at the current loop crossover frequency, f_{CI}, as shown in Figure 17 below.

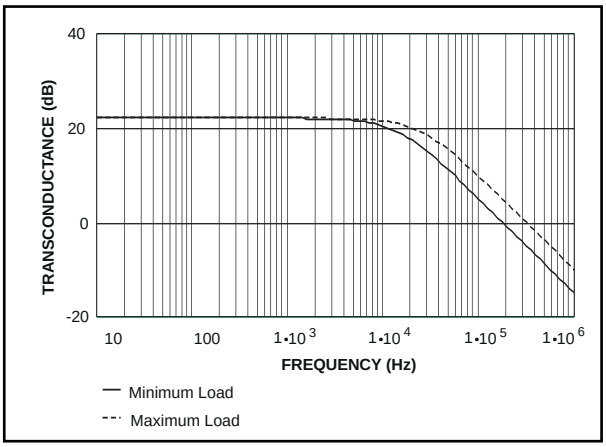

Figure 17. Small Signal Current Loop Transfer Function – Min and Max Loads

where the transconductance, TC(s) is determined by

$$T_{C(s)} = \frac{1}{R_S \bullet G_{CSA}} \bullet \left(\frac{1}{1 + \frac{s}{2 \bullet \pi \bullet f_{CL}}} \right)$$

The low frequency gain is the transconductance (remember, transconductance units is Ω^{-1})

$$Gain = \frac{1}{R_S \bullet G_{CSA}} = \frac{1}{0.01\Omega \bullet 7.87} = \frac{22.1dB}{\Omega}$$

Step 8: Determine the output impedance and power circuit gain, G_{Vs}.

The output impedance is determined by the output capacitance, its parasitics, and the load resistance.

$$Z_{Vout(s)} = \frac{\left(\frac{1}{s \bullet C_{OUT}} + ESR + s \bullet ESL \right) \bullet R_{LOAD}}{\left(\frac{1}{s \bullet C_{OUT}} + ESR + s \bullet ESL \right) + R_{LOAD}}$$

The power circuit gain equals the current loop transconductance times the output impedance, or

$$G_{Vs} = T_{C(s)} \bullet Z_{Vout(s)}$$

Step 9: Determine the gain required by the compensated voltage amplifier. Insure that gain at the switching frequency does not increase the PWM slope above the required amount due to ESR.

The resistors R14 and R16 around the voltage amplifier were determined by the requirements for non-integrating gain and are

$R14 = 15.0k\Omega$

$R16 = 100k\Omega$

The inductor current di/dt rate is known to be a maximum of 0.313A/µs. This inductor current ramp times the ESR of the output capacitor is multiplied by the gain of the voltage and current amplifiers and is seen at the PWM Comparator. The total contribution of ESR ripple contributed to the ramp at the PWM comparator is the limiting factor for the gain of the voltage amplifier, G_{VA}. Step 4 reduced G_{CAmax} by 25% to account for this factor. The gain of the Current Amplifier at the switching frequency, from Figure 16, is 3.3.

Therefore, from Step 4, and with an equivalent ESR of the output capacitors being 11.0mΩ

$0.313A/\mu s \bullet ESR \bullet (1+G_{CA(Fs)}) \bullet G_{VAmax(Fs)} = 0.25 \bullet 0364V/\mu s$

and therefore

$$G_{VAmax(Fs)} \quad \frac{0.25 \bullet 0364V/\mu s}{0.313A/\mu s \bullet 0.011 \bullet (1 + 3.3)}$$

$= 6.15$

Since R16 and R14 set an inverting gain of $100k\Omega/15k\Omega = 6.67$, then the voltage amplifier gain must be rolled off (add a pole) prior to the switching frequency to reduce the gain to less than $G_{VAmax(Fs)}$.

Step 10: Compensate the Voltage Amplifier to achieve desired loop gain and phase and to reduce the voltage amplifier gain at the switching frequency to below $G_{VAmax(Fs)}$.

The voltage loop gain is obtained by multiplying the power circuit gain, G_{Vs} by the Voltage Amplifier gain, G_{VAs}.

$$Loop V_S = G_{VAs} \bullet G_{Vs} = G_{VAs} \bullet T_{C(s)} \bullet \left(\frac{1}{s \bullet C_{OUT}} + ESR + s \bullet ESL\right) \bullet R_{LOAD}$$

$$\left(\frac{1}{s \bullet C_{OUT}} + ESR + s \bullet ESL\right) + R_{LOAD}$$

The voltage amplifier gain, without compensation, is simply R16/R14 = 6.67. The voltage loop gain is plotted in Figure 18, showing a very low crossover frequency.

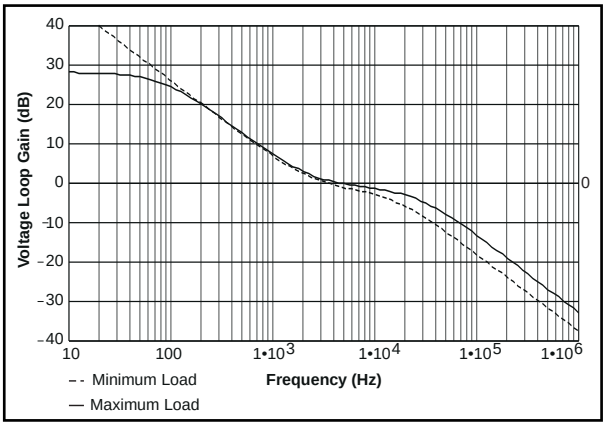

Figure 18. Voltage Loop Gain without Additional Voltage Amplifier Compensation

The voltage amplifier gain is compensated by adding a low frequency pole-zero pair in order to boost low frequency gain. Note however, that DC gain cannot be increased as it is limited by the requirements of non-integrating gain. Secondly, a high frequency pole is added to achieve the desired crossover frequency and to reduce the gain of the voltage amplifier beyond the crossover frequency.

Add C23 and R15 to add a low frequency pole-zero pair in order to boost low frequency (but NOT DC) gain, and therefore boost the crossover frequency. Set the zero at approximately 100Hz and the pole at approximately 400Hz.

The equations for the pole and zero are

$$F_{POLE} = \frac{1}{2 \bullet \pi \bullet C23 \bullet R15} \quad \text{and}$$

$$F_{ZERO} = \frac{1}{2 \bullet \pi \bullet C23 \bullet (R15 + R14)}$$

Set C23 to 0.1µF. Then

$$R15 = \frac{1}{2 \bullet \pi \bullet C23 \bullet F_{POLE}}$$

$$= \frac{1}{2 \bullet \pi \bullet 0.01\mu F \bullet 400} = 3.98k\Omega$$

Use R15 = 3.92kΩ as a standard value. The results are:

F_{POLE} = 406Hz
F_{ZERO} = 84Hz

Add C24 to add another pole to roll off the gain to obtain the desired crossover frequency and reduce the gain of the voltage amplifier at the switching frequency.

Set C24 to 180pF to obtain a pole frequency at

$$F_{POLE} = \frac{1}{2 \bullet \pi \bullet R16 \bullet C24}$$

$$= \frac{1}{2 \bullet \pi \bullet 100k\Omega \bullet 180pF}$$

$$= 8.84kHz$$

The transfer function for the compensated voltage amplifier is

$$GVA(s) = \frac{R16}{R14} \bullet \frac{s \bullet C23 \bullet (R14 + R15) + 1}{(s \bullet R16 \bullet C24 + 1) \bullet (s \bullet R15 \bullet C23 + 1)}$$

With this compensation, the voltage amplifier gain and the loop response for the Voltage Loop are plotted in Figure 19.

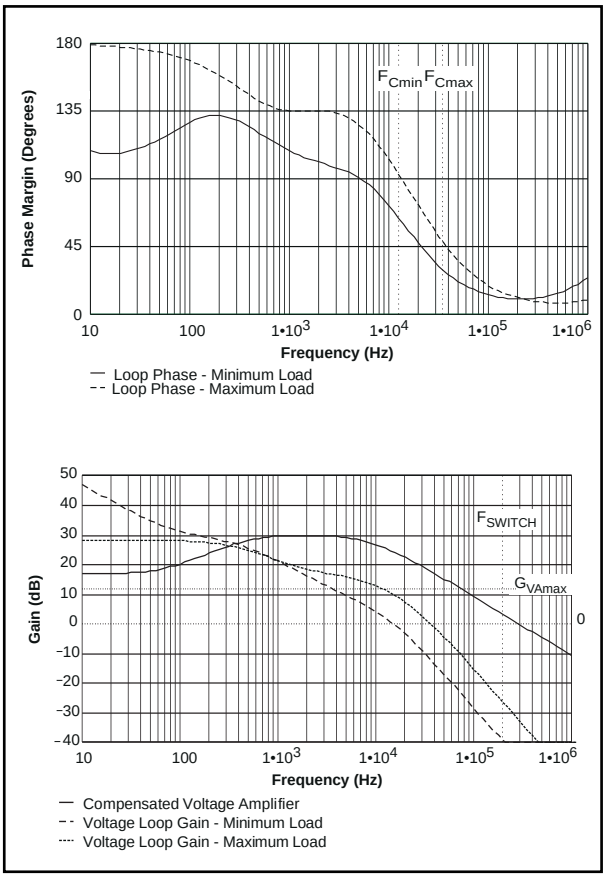

Figure 19. Final Voltage Loop Gain and Phase Plots

COMPONENTS Z1, R22 AND C26 CAN BE USED FOR VARIATIONS IN THE COMPENSATION SCHEME. THE VRM DEMONSTRATION KIT IS SHIPPED WITH Z1=10Ω AND WITHOUT R22 AND C26.

MEASURED RESULTS FROM THE VRM DEMONSTRATION KIT

Figure 20 provides the measured open loop response bode plots for the VRM power supply under a nominal 3.1V output at I_{Omax} = 11.2 Amperes.

Figure 21 shows the DC regulation measured at the load in a test configuration, with the nominal output voltage set to 3.100V. The measured test configuration DC impedance from the output of the connector to the resistive load is 1.50mΩ, which accounts for 17mV (0.54%) drop at full load. The load regulation curve matches the predicted non-integrating regulation curve.

Figure 22 shows the measured efficiency and power dissipation of the VRM in a test configuration, with the nominal output voltage set to 3.100V. The input voltage is fixed at 5.00V. The test board is subjected to 100LFM airflow at approximately 25°C ambient temperature. The full load efficiency is 83.6%.

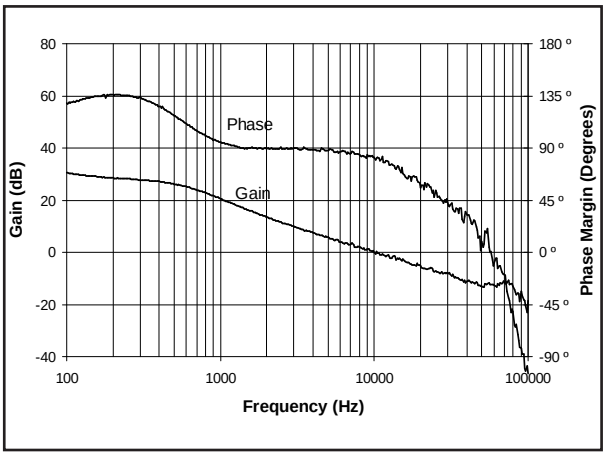

Figure 20. Open Loop Response with V_{OUT} = 3.1V, I_{OUT} = 11.2A

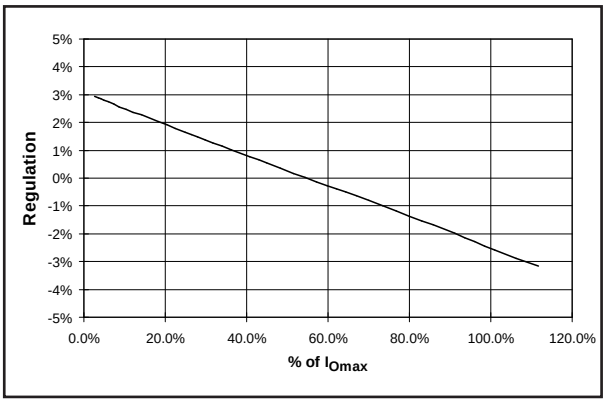

Figure 21. DC Regulation at V_{OUT} = 3.1V for VRM - Measured At Load

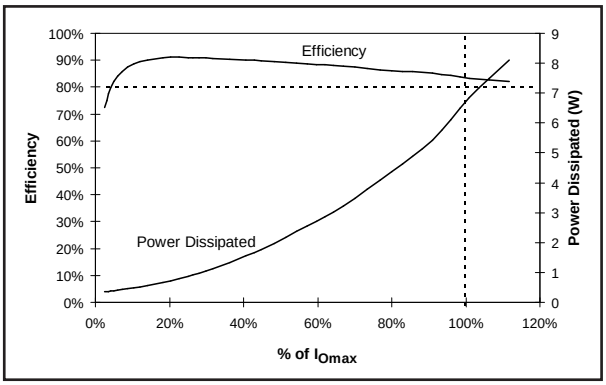

Figure 22. Efficiency and Power Dissipation vs Load for VRM Module with 3.100V nominal Output

The measured efficiency includes the power dissipated by the 12V bias power supply. The +12V current, I_{CC}, is measured to be 25.0mA during normal operation, and is fixed with varying load. With the OUTEN signal disabling the power supply, I_{CC} is measured at 18.5mA, supplying current only for the UC3886 and UC3910, but no gate drive. The average gate drive current is measured at 6.50mA.

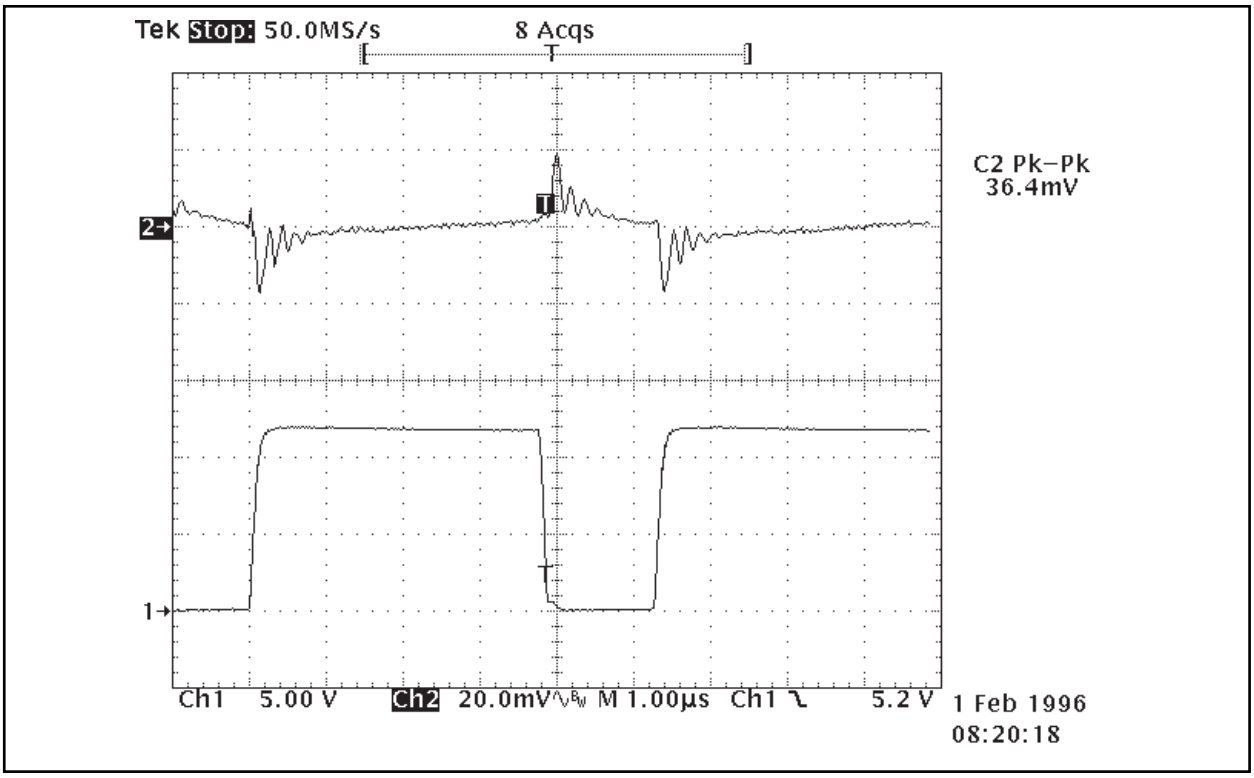

Figure 23. Ripple Voltage and Gate Voltage. V_{OUT} = 3.03V, I_{OUT} = 11.2A.

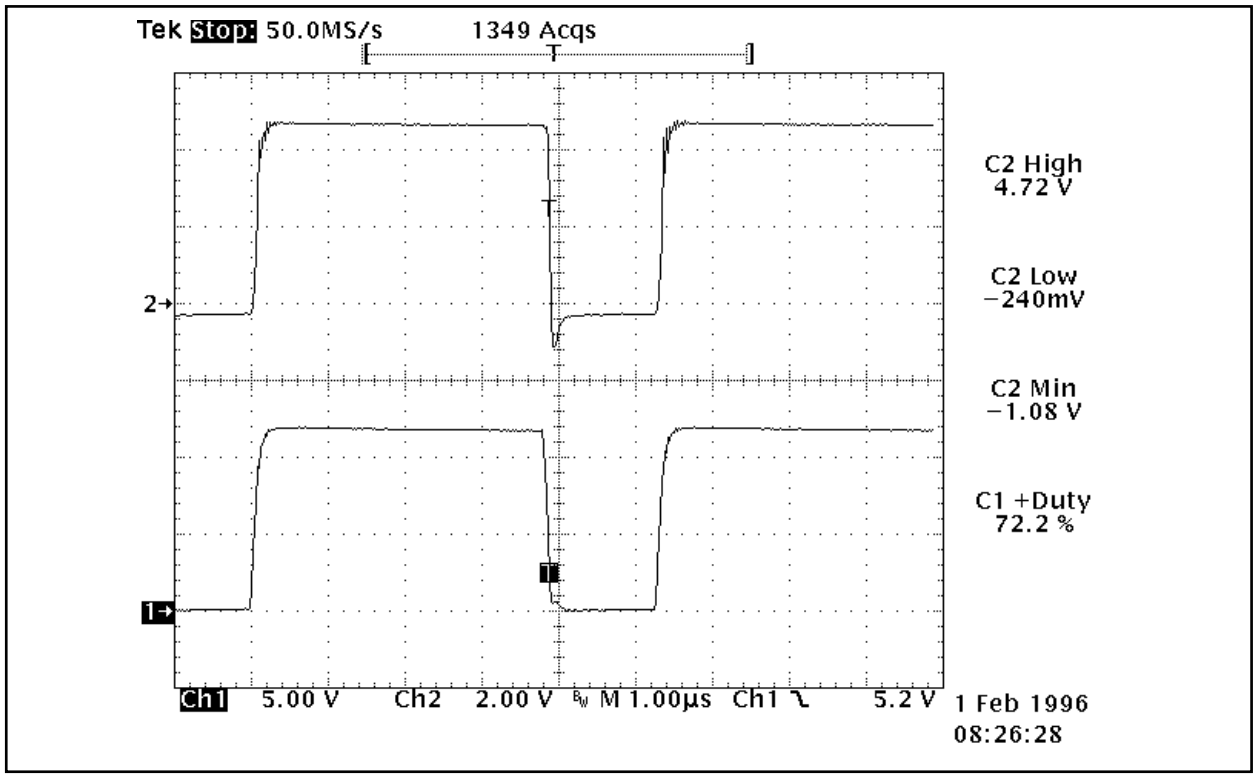

Figure 24. Source Voltage (Top) and Gate Voltage. V_{OUT} = 3.03V, I_{OUT} = 11.2A

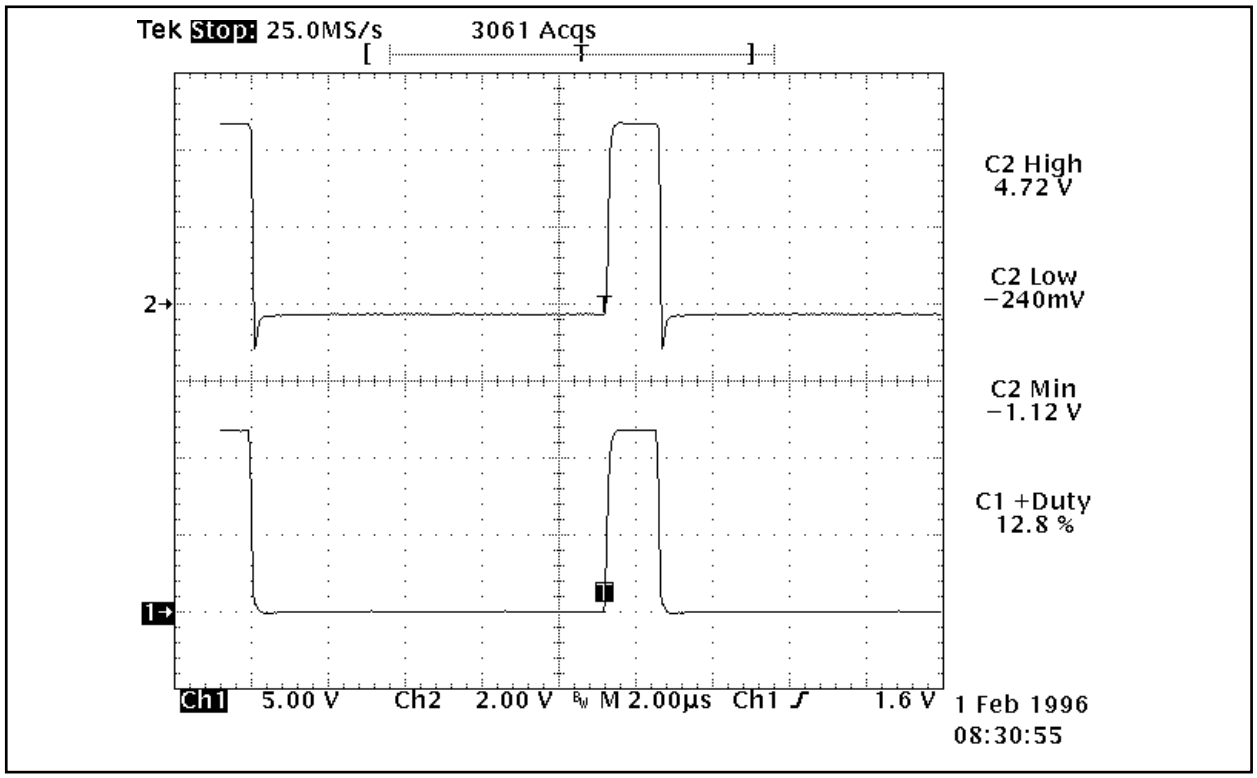

Figure 25. Short Circuit Source Voltage (Top) and Gate Voltage. V_{OUT} = 0.06V. The UC3886 skips cycles to maintain an accurate current limit.

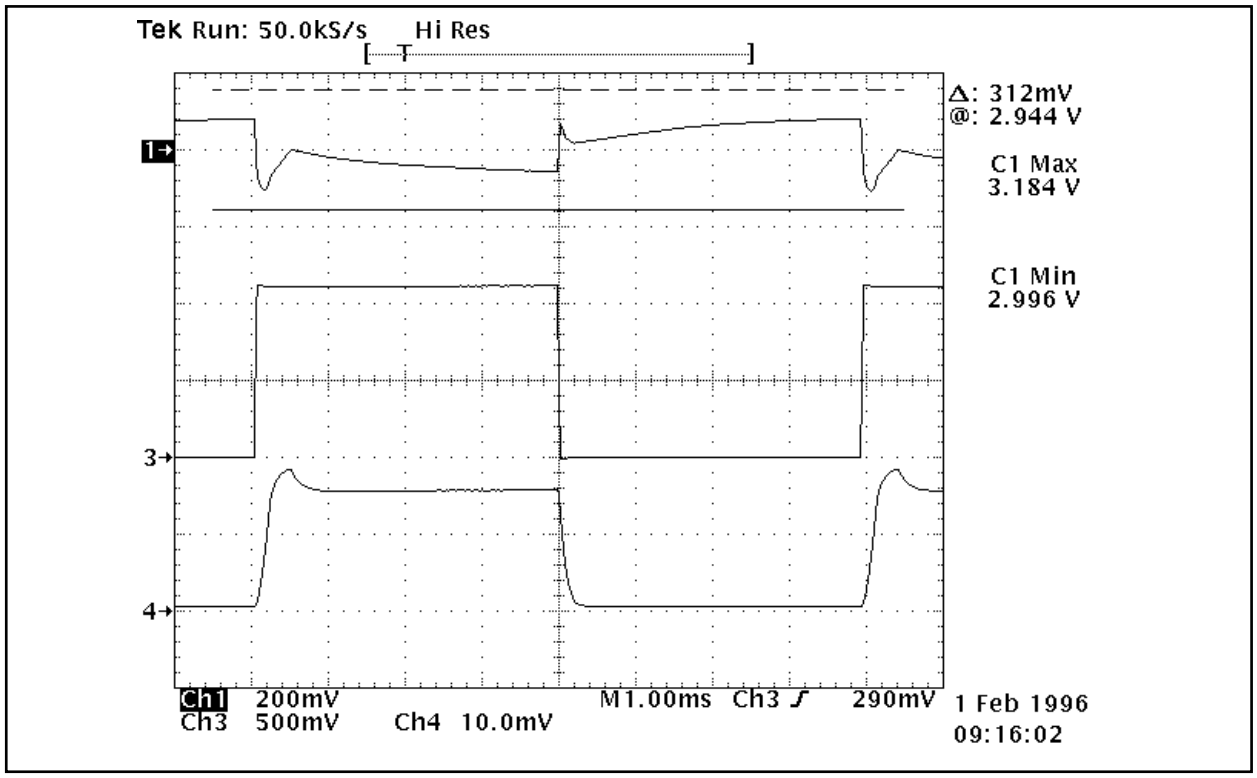

Figure 26. Transient Response to 125Hz, 0.3A to 11.2A to 0.3A Load Change. V_{OUT} (Top) centered about 3.10V, between ±5% cursors. Load current (Middle) @ 2A/div varies at 30A/µs. Input current (Bottom) @ 5A/div. overshoots to charge input and output caps after a load step.

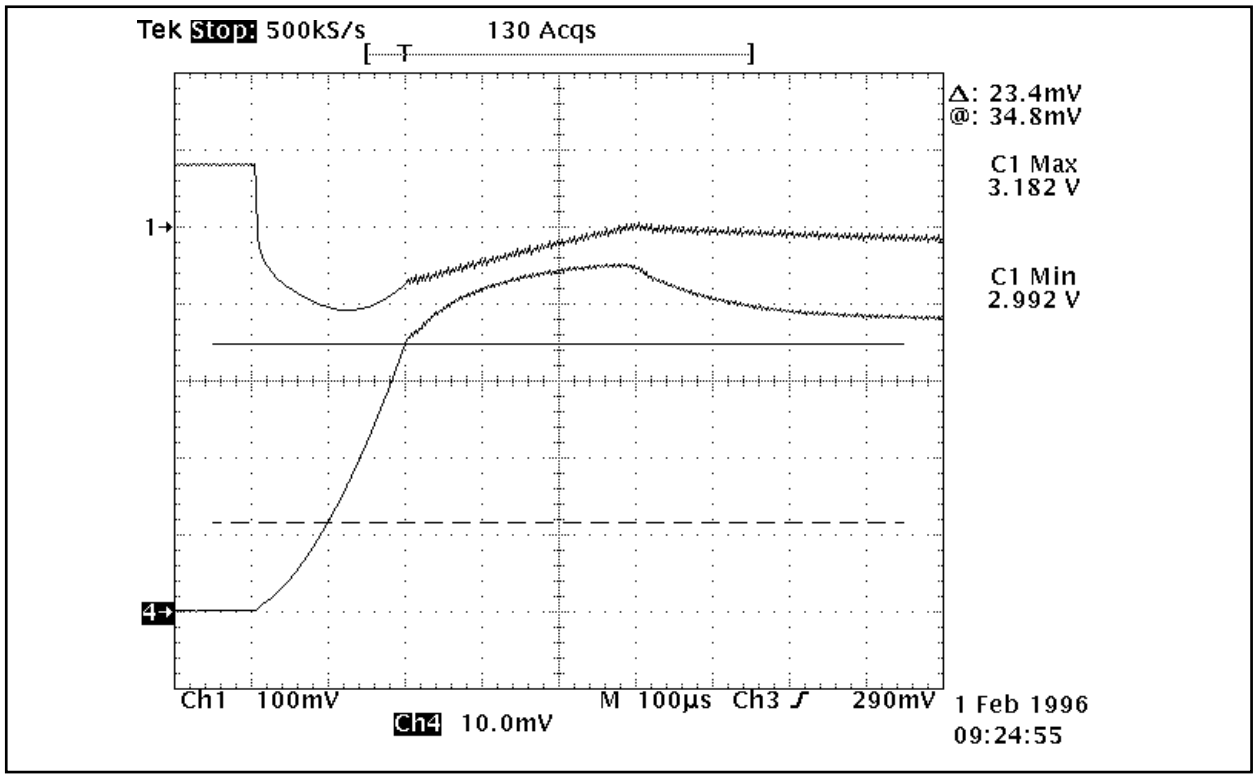

Figure 27. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 0.3A to 11.2A transient. Input current (Bottom, 2A/div) rises at 0.047A/µs during the load step.

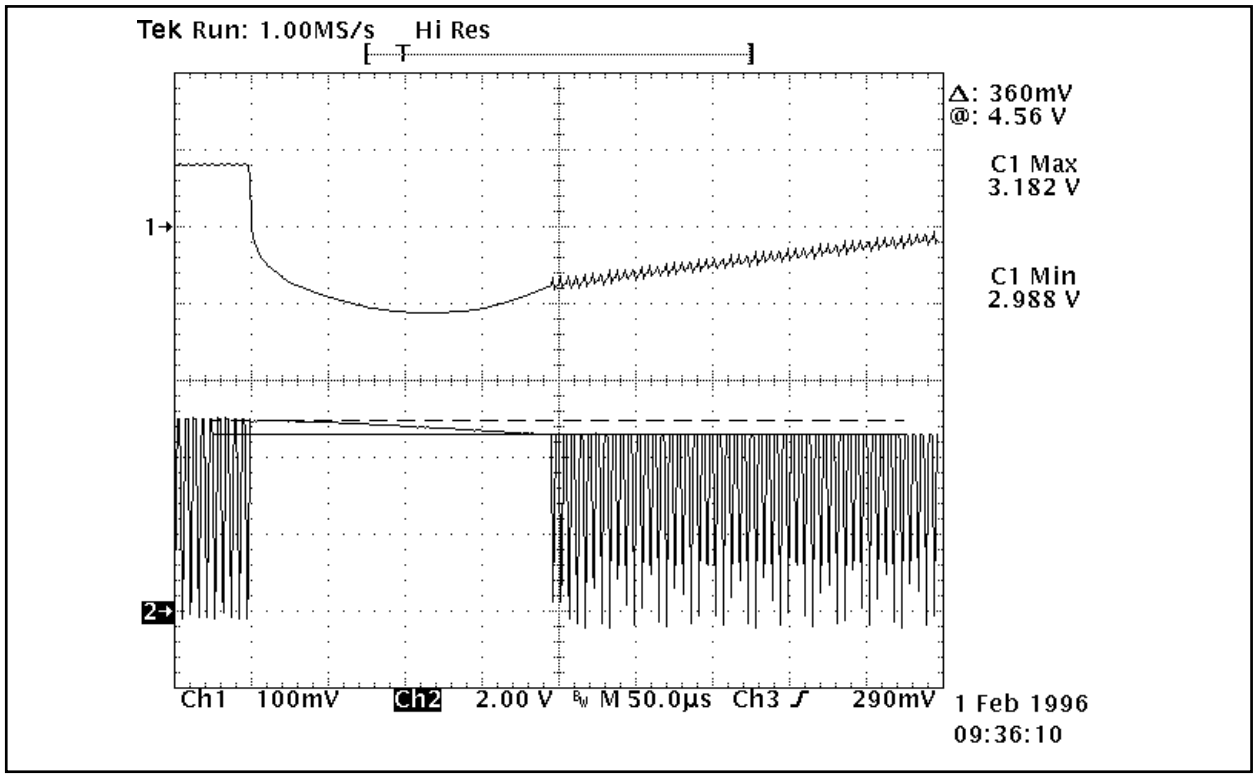

Figure 28. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 0.3A to 11.2A transient. Q1 Source (Bottom) shows 100% duty cycle as inductor current ramps to full load current. Slope in Source is due to Q1 R_{DSon}.

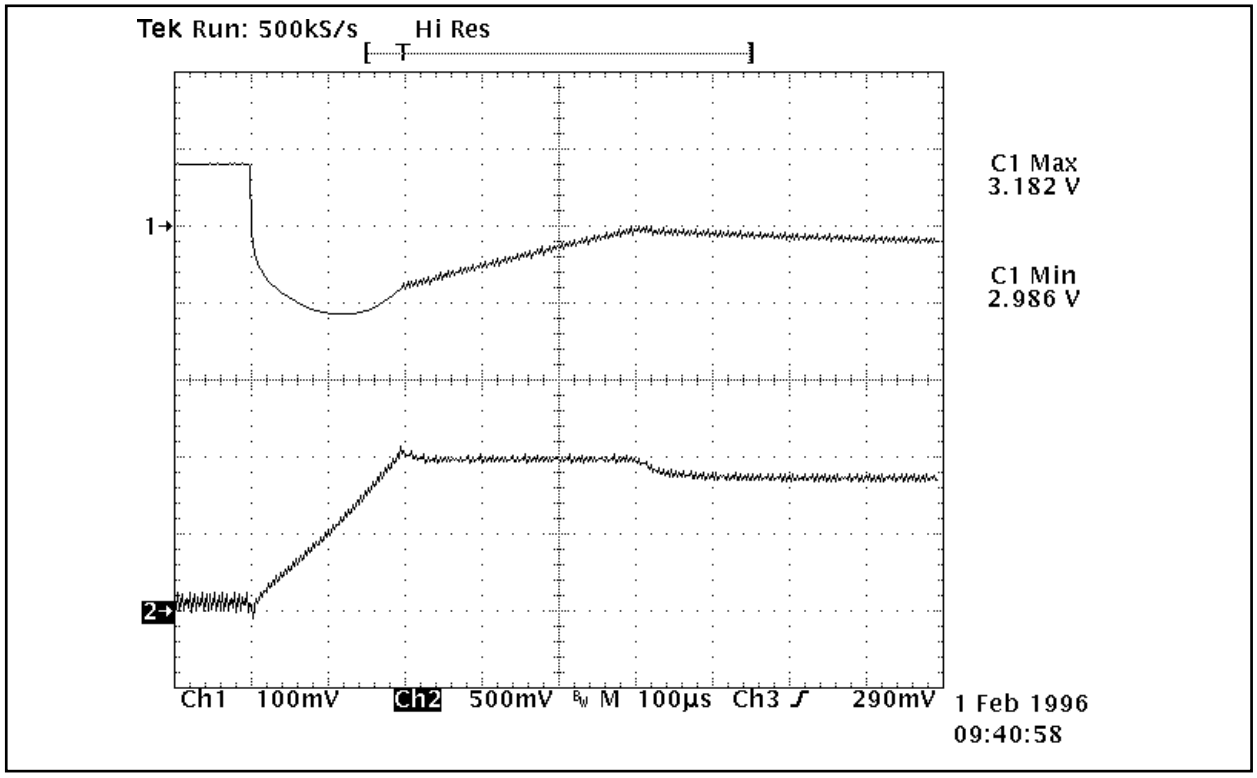

Figure 29. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 0.3A to 11.2A transient. ISO, UC3886 Pin 16 (Bottom) swings from 3.10V (Marker 2) to 4.10V at a measured 12.6A short circuit current. The output inductor is calculated to be 27µH during this swing due to high AC Flux.

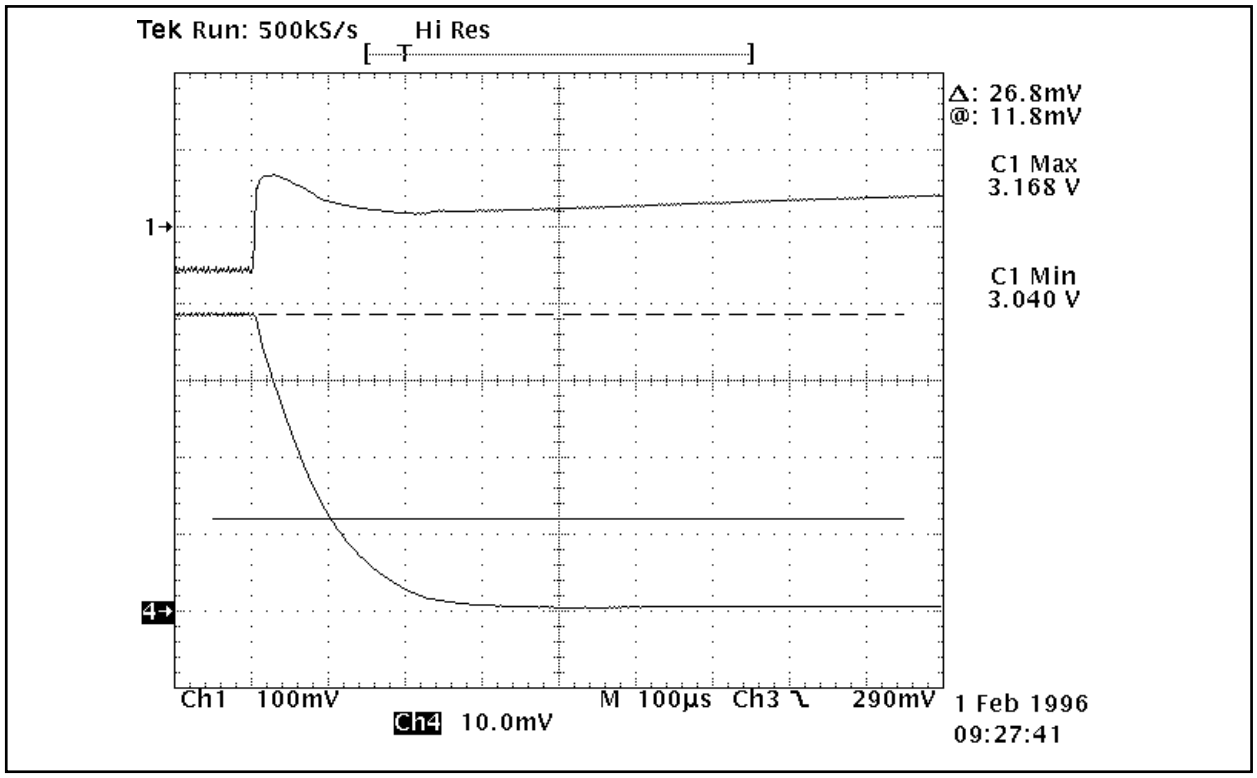

Figure 30. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 11.2A to 0.3A transient. Input current (Bottom, 2A/div) falls at 0.054A/µs during the load step.

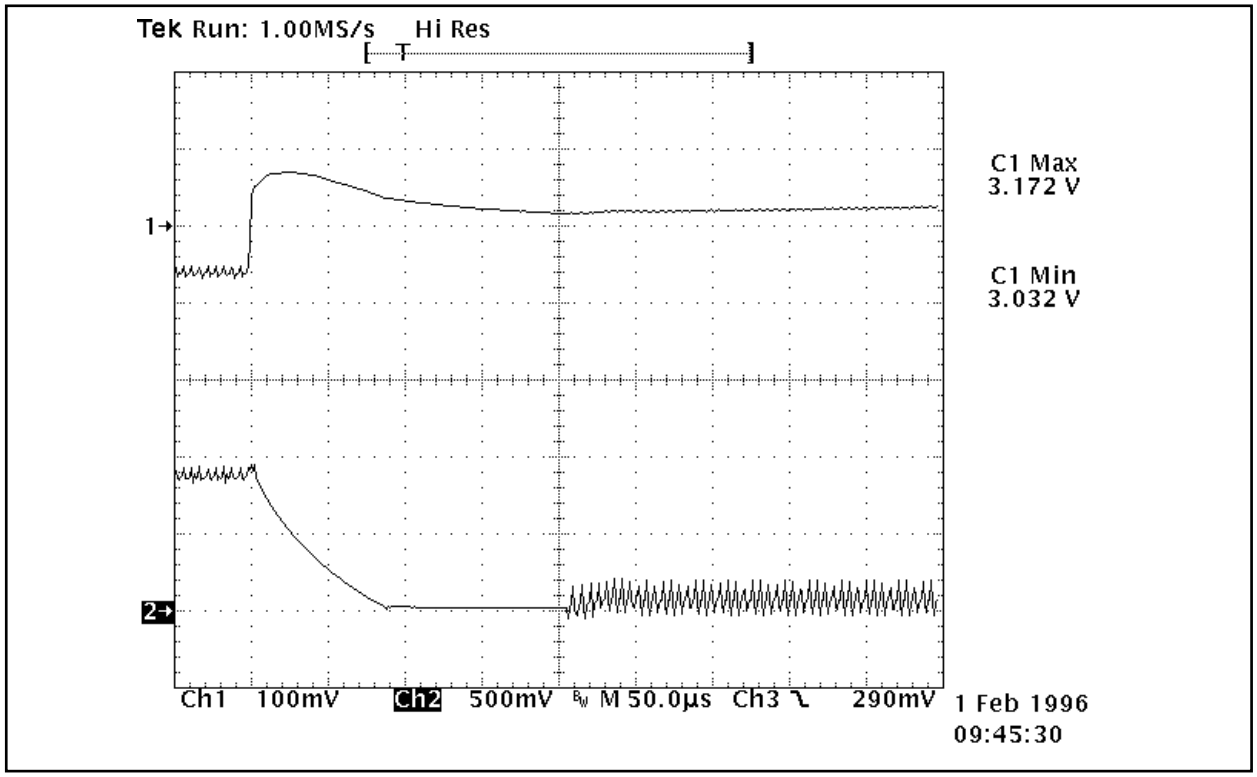

Figure 31. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 11.2A to 0.3A transient. ISO, UC3886 Pin 16 (Bottom) swings from 4.00V (Marker 2) to 3.10V. The output inductor is calculated to be 28uH during this swing due to high AC Flux.

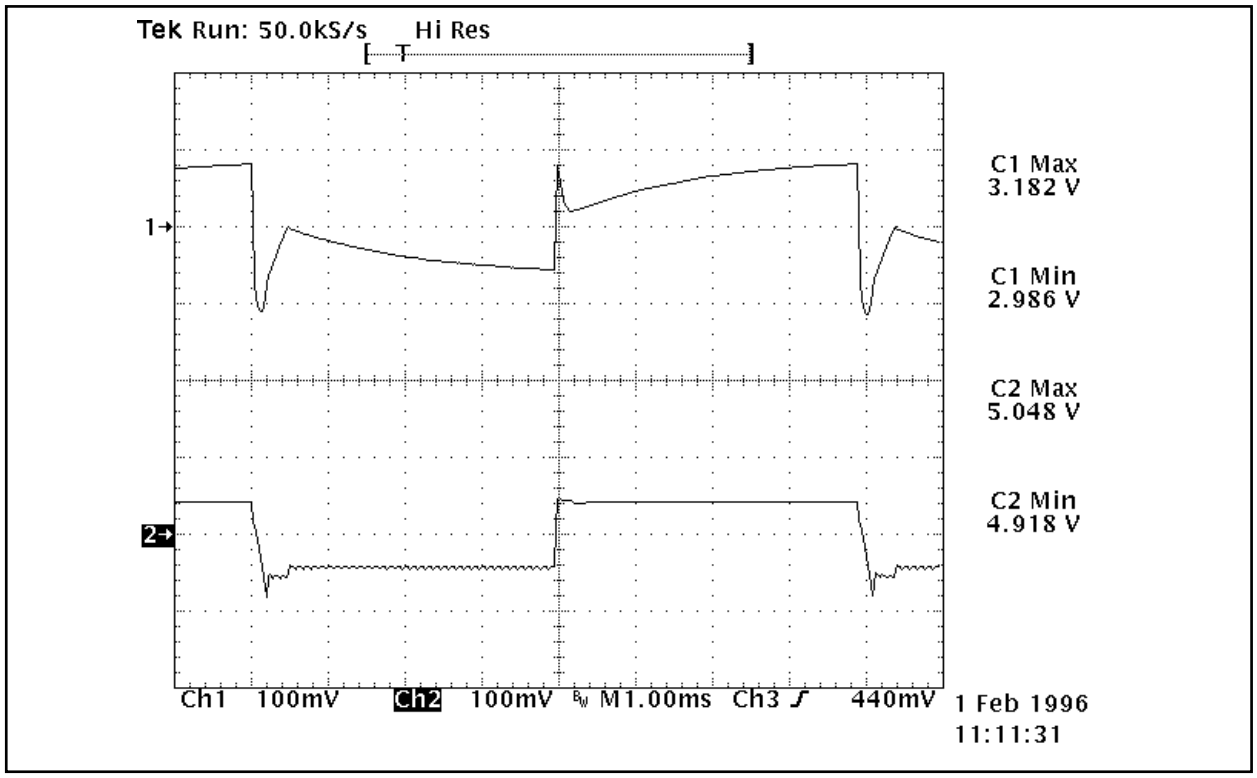

Figure 32. Transient Response to 125Hz, 0.3A to 11.2A to 0.3A Load Change. V_{OUT} (Top) centered about 3.10V. Input voltage (Bottom) shows only 130mV deviation during load steps without input inductor, due to low impedance VRM input capacitors.

CONCLUSION

A highly accurate VRM power supply has been demonstrated which uses Unitrode's UC3886 and UC3910 ICs. This VRM meets the Intel VRM power supply specifications, has excellent regulation, transient response, and efficiency. It has been demonstrated that a single output inductor can allow continuous mode operation, meet the stringent transient response of the Pentium®Pro, and limit the input current rate as well. The use of non-integrating voltage loop regulation has been proven to use fewer output capacitors because of the larger transient voltage swing allowed by this technique.

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